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Research Article

Analysis and Design of High-Energy-Efficiency Amplifiers for Delta-Sigma Modulators

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This study presents a dynamic amplifier with high energy efficiency and high gain suitable for a delta-sigma modulator based on the floating-inverter amplifier (FIA), in-depth analysis of the existing FIA and its improved structure, and simulation verification. Compared with other FIA structures, the proposed amplifier has a better compromise in terms of power consumption and stability, which was designed and simulated using the SMIC 180 nm CMOS technology. Under a 1.2 V power supply, the closed-loop direct current (DC) gain and the output swing were about 104 dB and ±380 mV, respectively, and the input-referred in-band noise was about −100 dB with the chopper circuit.

1. Introduction

With the outbreak of the Internet of things (IoT) sensing application market, analog-to-digital converters (ADCs) are the current research hotspot, especially high-energy-efficiency ADCs with high precision and high dynamic input swing. Different from bias low-power applications of SAR ADC [1] and towards the high-speed application of flash ADC [2], delta-sigma ADC is an excellent choice for energy-efficient ADCs because of its inherent high energy efficiency within the common bandwidth of the IoT.

The delta-sigma modulators are the main part of the delta-sigma ADCs. Amplifiers belong to the design core of the integrator in delta-sigma modulators, and their performance dominates the performance of the whole delta-sigma modulator. Therefore, high-energy-efficiency amplifiers have been a research hotspot in recent years. An inverter amplifier was proposed in [3] to achieve current reuse and large output swing. However, the gain was generally limited to about 30 dB and sensitive to the process, voltage, and temperature (PVT). In [4], a cascode inverter was proposed to achieve gain greater than 50 dB at the expense of swing, and it was still sensitive to PVT. A current-starved amplifier that adds a fixed current bias to combat PVT robustness but at the expense of swing was proposed in [5]. A dynamic bias amplifier which requires a complex common-mode (CM) feedback circuit was proposed in [6], increasing the design complexity and power consumption. A floating-inverter amplifier (FIA) and its application were proposed in [7, 8], which represents the highest energy efficiency level of the current amplifier design and has relatively good PVT robustness, but its gain was generally limited to about 30 dB. In [9], a cascode FIA was proposed to obtain a moderate gain by sacrificing a certain swing. A cascaded FIA was proposed in [10] to obtain a moderate gain and large output swing at the expense of power consumption. In some high precision and high-dynamic-range delta-sigma modulator applications, a medium gain may still not be sufficient. In addition, some gain-insensitive techniques have been proposed, such as correlated level shifting (CLS) [11, 12], averaging correlated level shifting (ACLS) [13], dynamic body-biasing (DBB)-assisted CLS [14], and a CLS technique with ping-pong operation [15]; they have been widely used in recent years but at the expense of area and clock circuit power consumption. In this study, the existing FIA techniques were analyzed and summarized in

detail and a high-gain FIA scheme was proposed, which has a better tradeoff between power consumption and stability.

Section 2 introduces the working principle of an FIA. In Section 3, in-depth analysis compares several structures with simulation verification. Section 4 introduces the high-gain FIA proposed in this study, and the simulation results and conclusions are given in Section 5.

2. Floating-Inverter Amplifier (FIA)

With the increasing demand for high-energy-efficiency amplifiers, researchers have made progress in the structural innovation of amplifiers year by year. The structure of the FIA was first proposed in [7], as shown in Figure 1. Its working process is divided into two stages: reset and amplification. In the reset stage, the energy storage capacitor (C_{RES}) is charged, while in the amplification stage, the amplifier is powered by the C_{RES}. In implementing current reuse at the same time, g_m/I_d increases as the overdrive voltage decreases in the amplification stage. Because of its high energy efficiency, it is widely used in some low-power applications.

Because of the particularity of the FIA's working principle, the C_{RES} will discharge continuously in the amplification stage, indicating that the power supply voltage of the amplifier keeps decreasing over time. Finally, the FIA will stop working when the voltage on the capacitor (V_{RES}) is less than the sum of the MOSFET threshold voltages ($V_{\mathrm{THN}} + V_{\mathrm{THP}}$) between the power and ground paths. At this time, the current of the amplifier is close to zero. This feature of the FIA is referred to as the self-quenched mechanism in [7]. This mechanism provides the amplifier extremely strong stability, and its open-loop gain has very low sensitivity to dynamic errors such as clock jitter. Compared with traditional closed-loop static amplifiers, the FIA does not need an additional CM compensation circuit because the FIA is powered by an C_{RES}. According to Kirchhoff's current law, the input and output currents of the C_{RES} must be equal, so there is no need for a complex CM feedback circuit [10].

3. Analysis and Simulation of Traditional FIA and Improved Amplifiers Based on the FIA

3.1. Low-Gain and Large-Swing FIA. The simple FIA structure is a unipolar point system whose small signal gain can be expressed as $\mathrm{A_V} = \mathrm{G_m R_o}$. The FIA's working current is provided by the $\mathrm{C_{RES}}$, which decreases with the discharge of the C_{RES}, so the analysis of the FIA's small signal model can only take the average value in a period of time. When FIA works at the beginning of the amplification phase, MOSFETs work in strong inversion due to sufficient charge on the $\mathrm{C_{RES}}$. Assuming that the transconductance of PMOS and NMOS is the same, the average expression of the FIA transconductance is shown in the following formula:

$$G_{m,\mathrm{avg,si}} = \frac{8C_{\mathrm{RES}}}{T_s} \ln\left(1 + \frac{T_s}{2\tau_{0,\mathrm{si}}}\right), \tag{1}$$

where

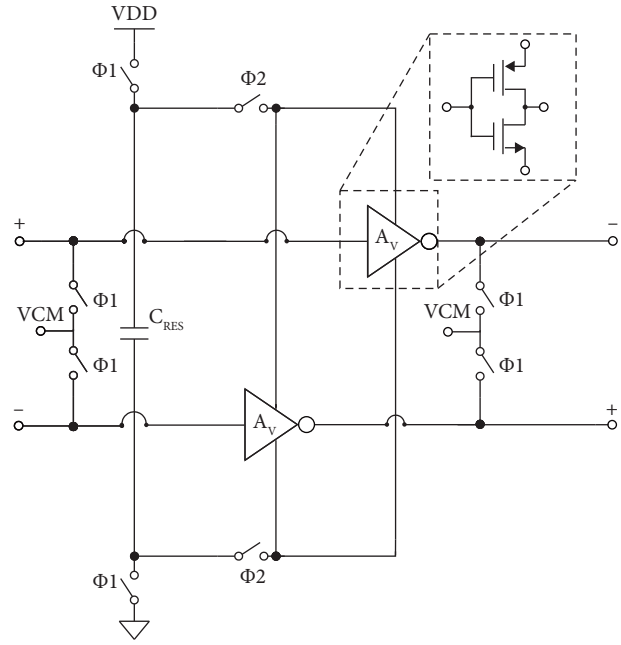

Figure 1: Structure of FIA.

$$\tau_{0,\mathrm{si}} = \frac{2C_{\mathrm{RES}}}{G_{m,0,\mathrm{si}}}, \tag{2}$$

where T_s is a working period of FIA and $G_{m,0,\mathrm{si}}$ is the transconductance of the MOSFET working in the strong inversion at the beginning of the amplification phase [7]. If the C_{RES} is large enough, $\tau_{0,\mathrm{si}} \gg T_s/2$, then the amplifier will behave as if it were powered by an ideal voltage source, where the average small signal transconductance $G_{m,\mathrm{avg,si}} \approx 2G_{m,0,\mathrm{si}}$. However, the C_{RES} in the actual circuit cannot be infinite, so with the continuous discharge of the C_{RES}, MOSFETs will work in the weak inversion for a period of time before switching off, and the expression of the FIA average transconductance is as follows:

$$G_{m,\mathrm{avg}} \approx \frac{8C_{\mathrm{RES}}}{T_s} \ln\left(\frac{T_s}{2\tau_{0,\mathrm{si}}}\right), \tag{3}$$

which is assumed that the FIA working time in the strong inversion area is much longer than that in the weak inversion area [7]. The above analysis applies to simple FIA and cascode FIA, where the small signal transconductance of FIA architecture as an amplifier is not a constant. Different from traditional amplifiers, due to the characteristics of FIAs' $\mathrm{C_{RES}}$ power supply, the working current of FIA will continue to decrease with the discharge of C_{RES}, resulting in an increase in the output impedance of MOSFETs and a decrease in the pole frequency of FIA. As a result, the simulation results of the gain over frequency and phase over frequency of FIA cannot well reflect the performance of FIA. In this paper, the variation trend of unity-gain bandwidth (UGB) and phase margin (PM) over time is adopted to represent the working state of these FIA-based amplifier structures. The simulation results of the low-gain and large-swing FIA are shown in Figures 2 and 3.

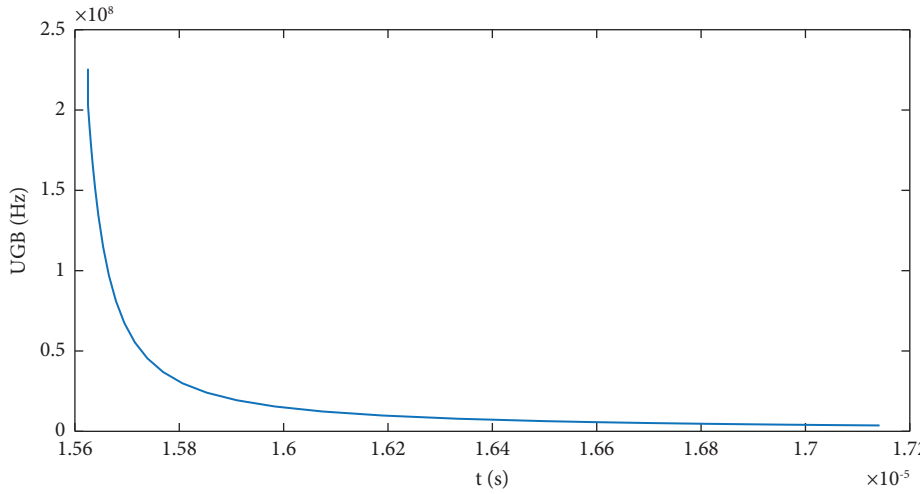

Figure 2: Time varying UBG of the simple FIA structure.

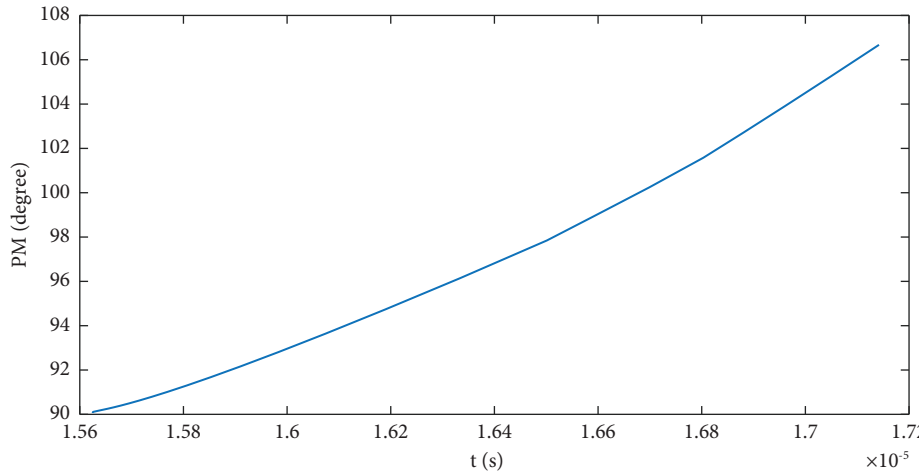

Figure 3: Time varying PM of the simple FIA structure.

According to [9], the input-referred in-band noise of the structure is $\overline{v_{n,i}^2} \approx kT/C_{in}$. At the same time, the unity-feedback structure mentioned in [9] was used, as shown in Figure 4. At a sampling frequency of 128 kHz and a bandwidth of 0.5 kHz, transient noise was added to obtain the normalized equivalent input noise, as shown in Figure 5, and the sigma value was about −93.40 dB. For the sake of simplicity, the later noise analysis was performed under this condition.

3.2. Medium-Gain and Small-Swing FIA. The closed-loop direct current (DC) gain of the integrator using a simple FIA can only reach about 30 dB in general, which is not suitable for high-precision delta-sigma modulator applications. Therefore, an improved FIA with a higher gain has been reported, whose structure was proposed in [9]. The circuit structure is shown in Figure 6. Because of the high output impedance of the cascode structure, a higher gain $A_V = (G_m R_o)^2$ is achieved, which can generally reach more than 60 dB, but it requires additional bias voltage or MOSFETs with different size ratios. At the same time, because of the cascode structure, the output swing is limited, making the structure only suitable for some applications with a medium gain and low output swing.

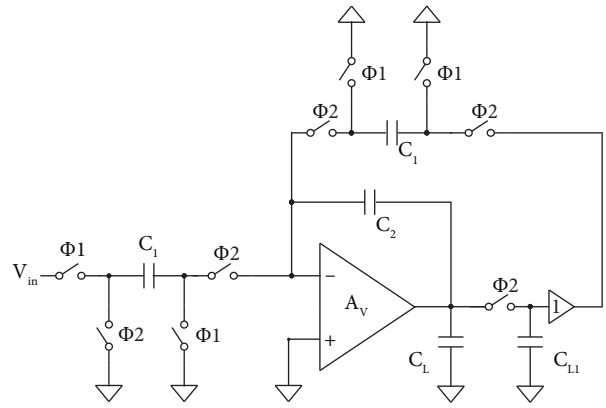

Figure 4: Switching capacitance (SC) integrator with unity feedback.

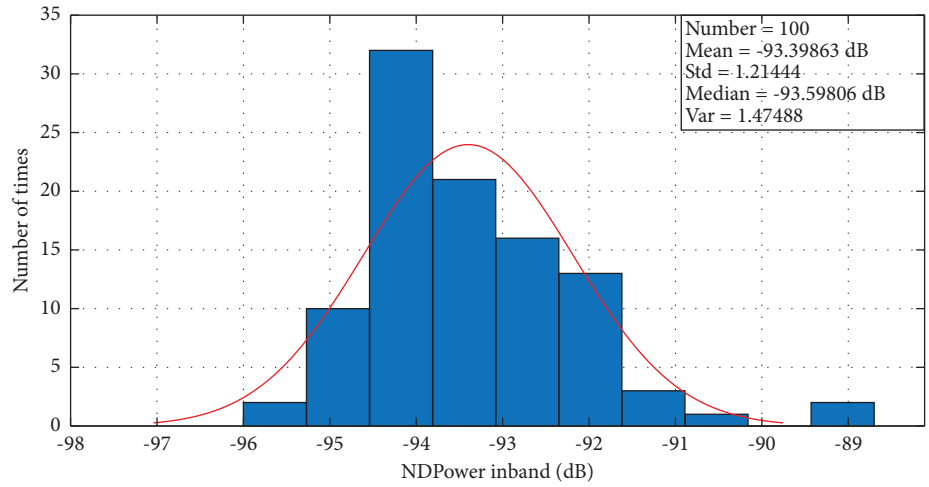

Figure 5: Histogram of the normal distribution of the input noise of the FIA (Number: number of simulations, Mean: mean value, Std: standard deviation, Median: median value, Var: variance, and Mean: mean value).

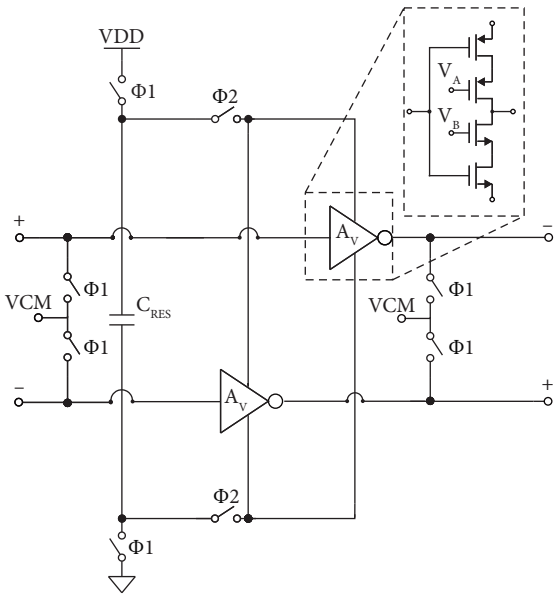

Figure 6: Cascode FIA structure.

Because the high output impedance of the cascode structure yields a high gain and the UGB of the unipolar system is mainly related to the current, the change in the pole frequency caused by the discharge of the same size, the C_{RES} has little effect on the PM. From the simulation results in Figures 7 and 8, the UGB of the proposed structure is similar to that of the structure in Figure 1, while the PM slightly changes. According to [9], the input-referred in-band noise of this structure is similar to that of the structure in Figure 1. The transient noise simulation results of this structure are shown in Figure 9, and the sigma value is about −93.34 dB. The simulation proves that the input-referred in-band noises of the two structures are basically similar under the same energy storage capacitance.

3.3. Cascaded Medium-Gain and Large-Swing FIA. Although the cascode FIA has a medium gain, it sacrifices part of the output swing. To solve the contradiction between the single-stage FIA gain and output swing, a cascaded structure of the simple FIA was proposed in [10], as shown in Figure 10. Sufficient output swing can be guaranteed for the amplifier when cascaded gain of a two-stage simple FIA is achieved.

Its working process can be divided into reset and amplification stages. First, in the reset stage ($\Phi1 = 1$ and $\Phi2 = 0$), the input and output voltages of the amplifier are reset to the CM voltage V_{CM}. At the same time, the C_{RES} starts precharging and quickly charges to the power supply voltage to prepare for the dynamic amplification of the next phase. With diameters of $\Phi1 = 0$ and $\Phi2 = 1$ in the amplification stage, the upper and lower plates of the C_{RES} are connected to the power supply track of the amplifier so that the amplifier can be started to work. Because the output CM voltage will be reset back to the CM voltage at the beginning of each cycle and the enabled switch timing of the two stages of the amplifier is the same, the closed-loop amplification function is realized. The structure consumes more power and area to achieve a medium gain.

The equivalent noise model of the two-stage amplifier based on the FIA is shown in Figure 11. According to the analysis in [10], the equivalent input-referred in-band noise expression of this structure is

$$\overline{v_{n,i}^2} \approx \frac{kT}{C_F \cdot C_{\text{Total}}/C_F + C_S} \cdot G_{m2} R_{O1}. \tag{4}$$

Because the C_{RES} of the second stage is designed to be smaller than that of the first stage, the noise factor will gradually decrease as the working current of the second stage decreases faster, so the amplification effect of the noise factor $G_{m2}R_{O1}$ on the input-referred in-band noise of the first stage will also gradually decrease.

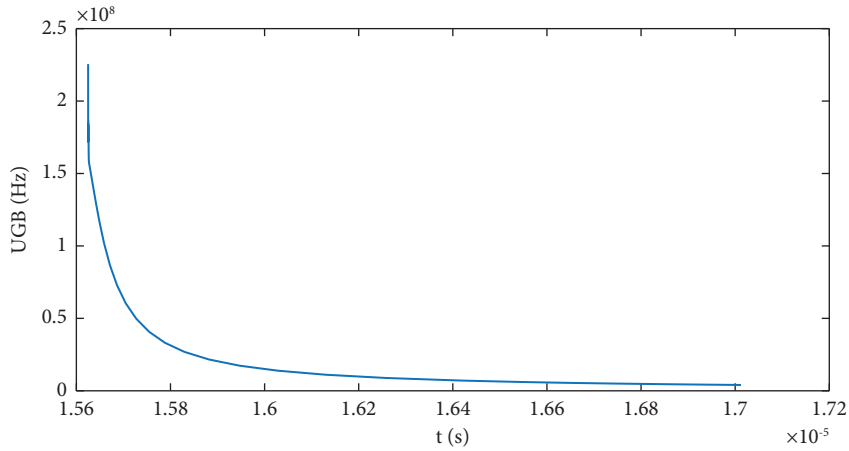

Figure 7: Time varying UBG of the cascode FIA structure.

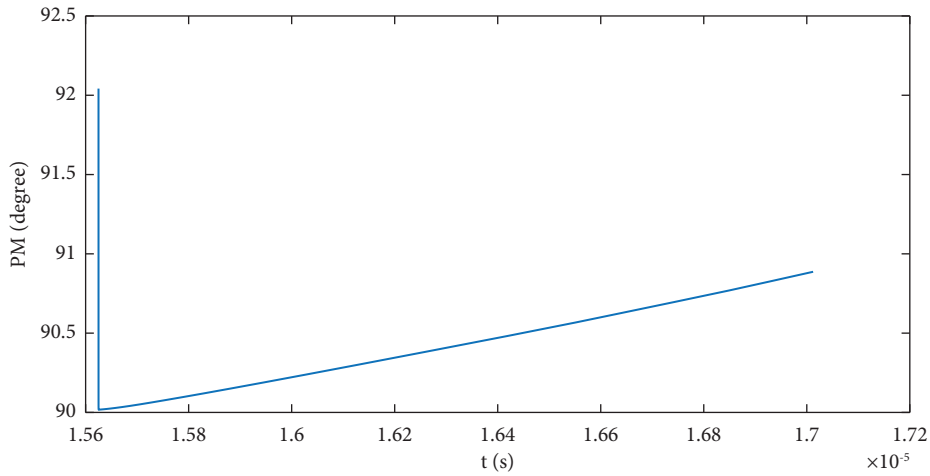

Figure 8: Time varying PM of the cascode FIA structure.

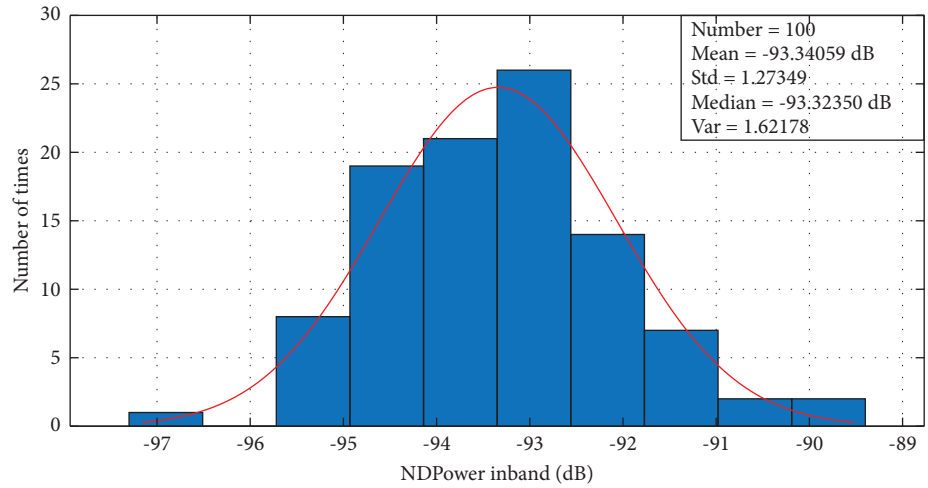

Figure 9: Histogram of the normal distribution of the input noise of the cascode FIA.

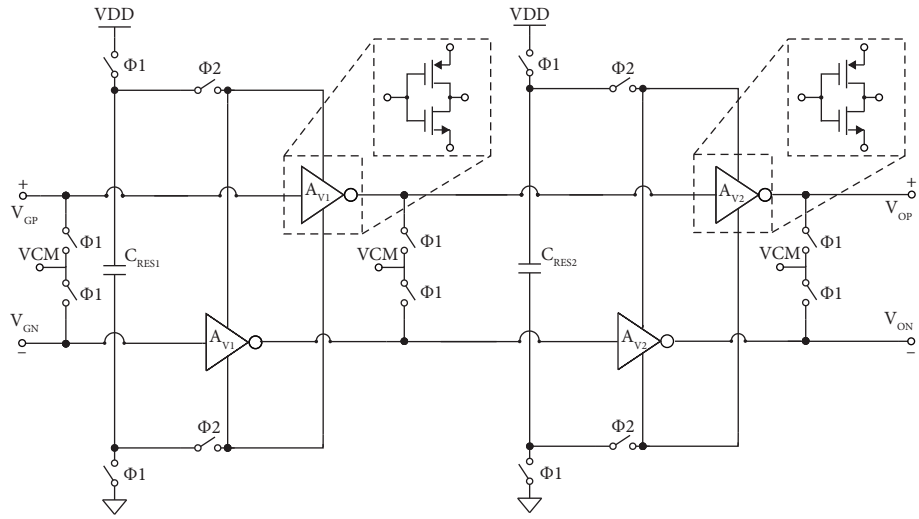

Figure 10: Two-stage FIA structure.

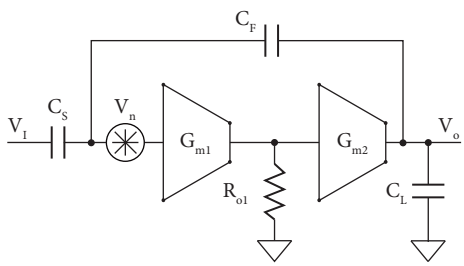

Figure 11: Noise model of the two-stage amplifier.

According to (2), compared with the single-stage FIA input noise analyzed earlier, the cascaded FIA input-referred in-band noise generated by the first-stage amplifier is amplified by the noise factor $G_{m2}R_{O1}$, so the noise performance will be decreased.

As shown in Figure 12, the sigma value of the structure is about −87.06 dB. Compared with the simulation results earlier, the noise performance of the two-stage FIA will decrease significantly, which is consistent with the theoretical analysis.

3.4. Cascaded High-Gain and High-Input-Range FIA. Although the two structures shown in Figures 6 and 10 achieve a closed-loop DC gain of greater than about 60 dB, it is still not enough to meet the design requirements of some applications with high precision and high dynamic range. To achieve a greater gain, an improved two-stage amplifier based on the FIA was proposed in [16], as shown in Figure 13. The first stage adopts the cascode FIA, and the second stage still uses a simple FIA, which achieves a high gain and still has a large output swing, but the structure is analyzed according to (2). The high output impedance of the first stage provided by the cascode structure will increase the noise factor $G_{m2}R_{O1}$. As a result, the noise performance of the structure is greatly sacrificed. At the same time, due to the large output load capacitance and the high output impedance of the first stage, it is necessary to add an additional compensation capacitor at the output of the first stage for the stable operation of the circuit. This structure does not have the condition of a single variable, so this study does not conduct in-depth analysis and simulation of this structure.

4. Two-Stage High-Gain FIA

For cascade integrators with a feedforward structure commonly used in delta-sigma ADCs, due to the input feedforward path and the dynamic range scaling of the integrator outputs [9], the structure does not require a high integrator output swing but a high amplifier gain in applications with high precision and high dynamic range. On the basis of this application scenario, in this study, a novel two-stage amplifier based on the FIA structure was proposed, as shown in Figure 14. The cascode structure was used in the second stage, which has a larger output impedance and makes the amplifier have a high gain. The operating principle is the same as that of the two-stage closed-loop amplifier shown in Figure 1.

The unity-gain integrator ($C_S = C_F$) was constructed with a switching capacitor, as shown in Figure 15. Simulation tests of the DC gain and output range were conducted when the power supply voltage was 1.2 V. The DC gain simulation results of the integrators with different structures at varying output voltage under the same energy storage capacitance are shown in Figure 16. The simulation results are consistent with the DC gain and output range of the three structures in the above analysis. A simple FIA and a two-stage FIA are appropriate for large-input-swing applications. The proposed FIA + cascode FIA is the most appropriate when the demand for a high gain and high dynamic range is high, and the output swing of the integrator is not high.

The new amplifier proposed in this paper has the same working principle as several structures mentioned above, and the relationship between its small signal transconductance and energy storage capacitance is still complex with the derivation mentioned above, so it will not be

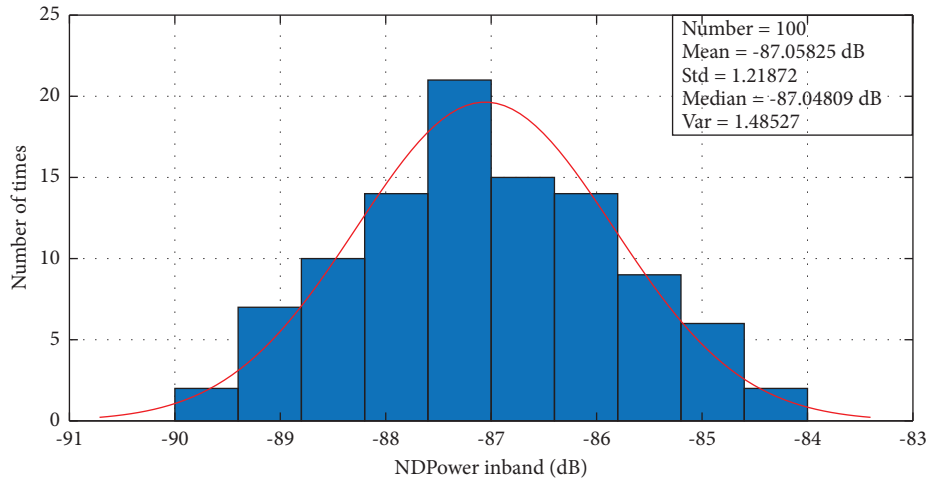

Figure 12: Histogram of the normal distribution of the input noise of the cascaded FIA.

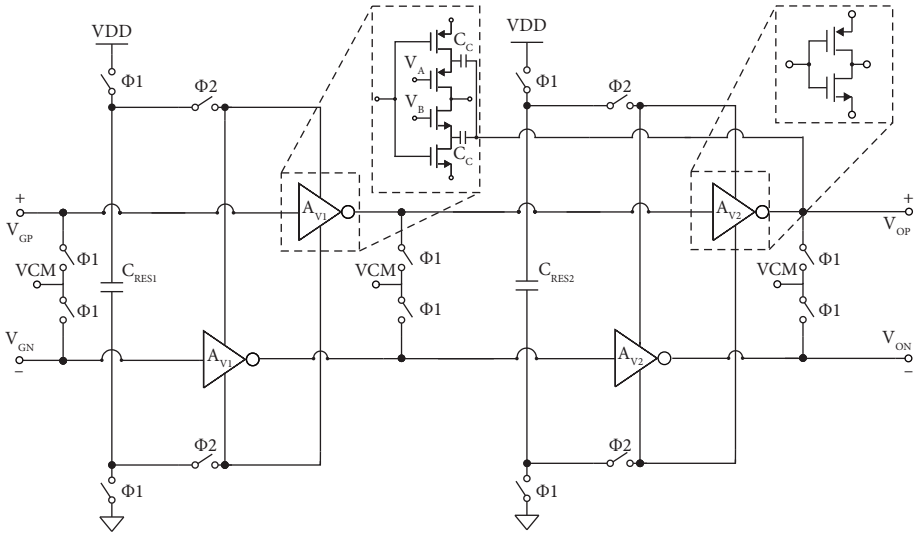

Figure 13: Two-stage high-gain FIA structure with a compensation capacitor.

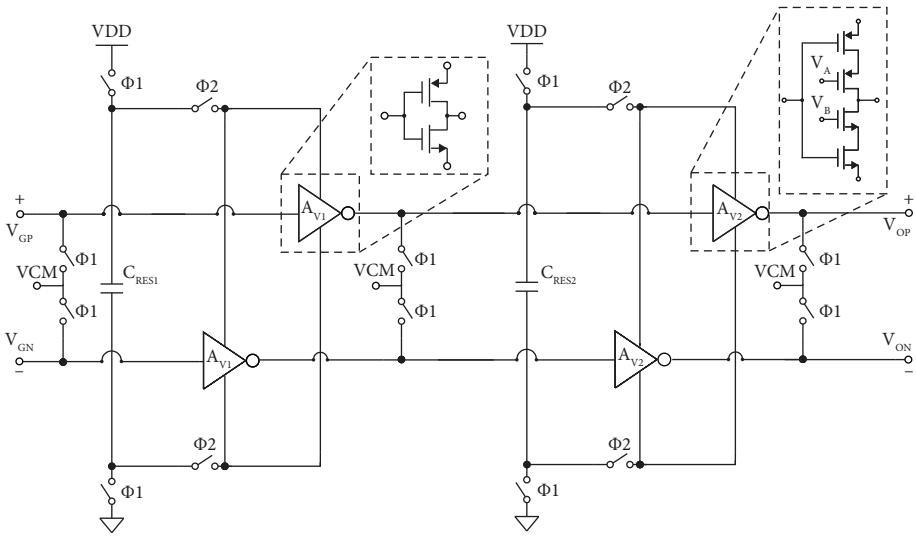

Figure 14: Two-stage high-gain FIA structure.

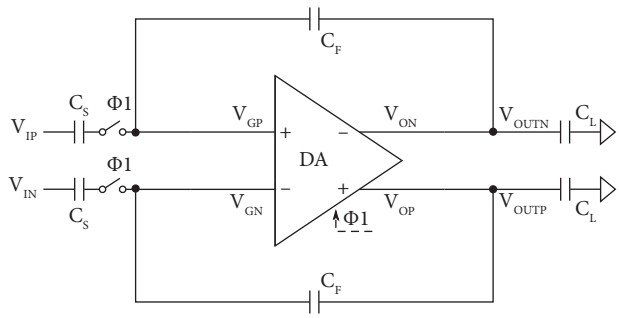

Figure 15: Unity-gain SC integrator.

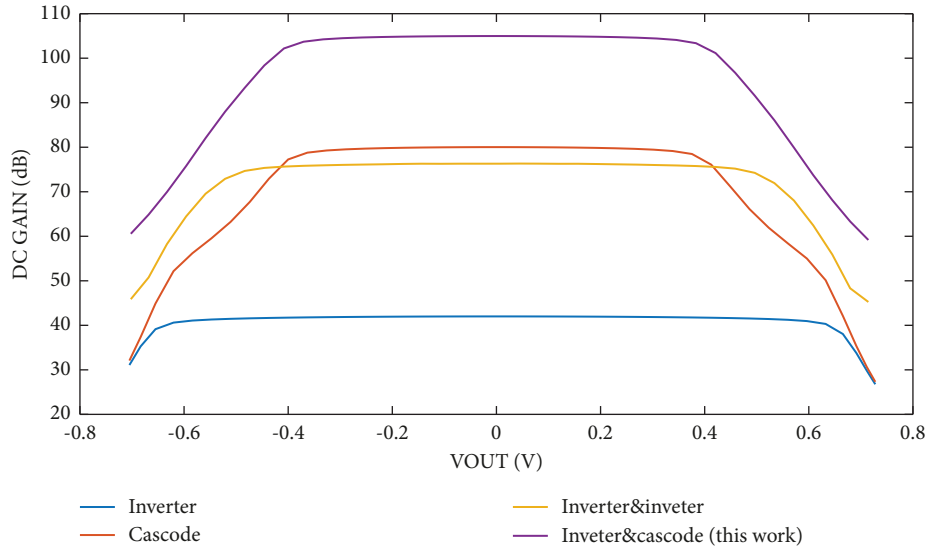

Figure 16: DC gain varying with output voltage (inverter: the structure in Figure 1, cascode: the structure in Figure 6, inverter and inverter: the structure in Figure 10, and inverter and cascode: the structure in Figure 14).

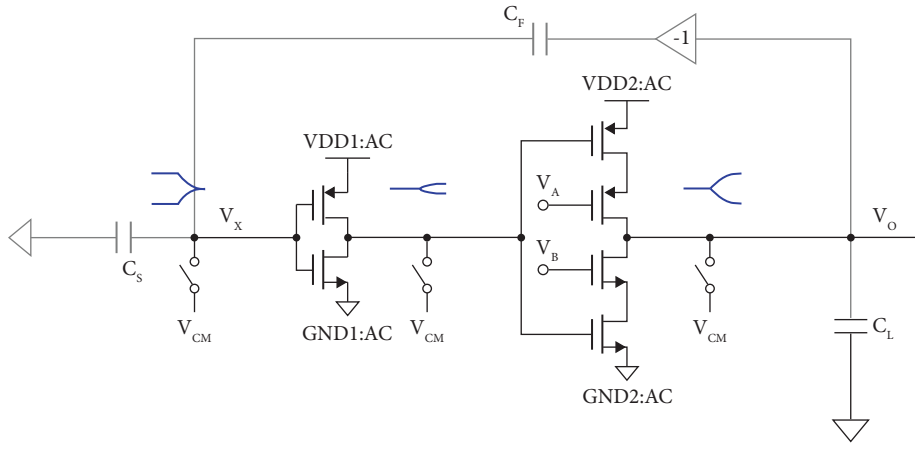

Figure 17: Equivalent single-ended AC model with negative feedback.

repeated here. Since the two-stage amplifier is enabled at the same time, a negative feedback circuit can be introduced to form a closed-loop amplifier and realize the function of closed-loop amplification. The signal change process of the closed-loop amplifier is shown in Figure 17.

For a two-stage dynamic amplifier, stability must be considered. In a traditional two-pole system, to obtain a sufficient PM, the frequency of the nondominant pole is often designed to be more than twice that of the UGB, increasing power consumption. The two-stage dynamic

amplifier proposed in this study is also a two-pole system. The two poles are the output nodes of the first and second stages of the operational amplifier, but the amplifier designed in this study can work stably without an additional compensation capacitance.

According to the analysis of the pole frequency of the two-stage FIA in [10], the pole frequency is $f = 1/R_oC_o$, where C_o is the output load capacitance and R_o is the output impedance; the output impedance of a MOSFET is $r_o = \partial V_{ds}/\partial I_{ds} = 1/g_{ds}$. According to the equivalent output impedance analysis diagram of the first and second stages shown in Figure 18, the output impedance of the first stage is expressed as $R_{O,1} = 1/(g_{ds,p} + g_{ds,n})$, while that of the second stage is expressed as follows:

$$R_{O,2} = \frac{g_{m,p2} \cdot g_{m,n2}}{\left(g_{m,n2} \cdot g_{ds,p1} \cdot g_{ds,p2}\right) + \left(g_{m,p2} \cdot g_{ds,n1} \cdot g_{ds,n2}\right)}, \quad (5)$$

where $g_{m,p2}$ and $g_{m,n2}$ are the equivalent transconductance of common-gate PMOS and NMOS, respectively. At the same time, because of the large output load capacitance of the second stage, the second-stage output pole must be the dominant pole.

Different from traditional amplifiers, because the C_{RES} of the FIA will discharge in the amplification stage, the current in the amplifier will decrease with time, resulting in increasing output impedance, which will lead to the change in pole frequency. Therefore, the C_{RES} of the second-stage FIA was designed to be smaller than that of the first-stage FIA ($C_{RES1} = 33$ pF and $C_{RES2} = 6$ pF), making the discharge rate of the second-stage amplifier higher, and the frequency variation of the dominant pole was greater than that of the nondominant pole, thus increasing the PM; thus, the amplifier can work stably without the need of an additional compensation circuit.

From Figures 19 and 20, the UGB of the amplifier starts from 900 MHz, indicating that the C_{RES} provides a great working current to the amplifier at the beginning of the amplification stage. Later, as the C_{RES} continues to discharge over time, the current keeps decreasing, so the UGB gradually decreases. As the C_{RES} of the first stage is larger than that of the second stage, the frequency of the dominant pole decreases faster than that of the nondominant pole. The initial PM is 33° and the final PM is close to 87°, showing that the output waveform of the closed-loop amplifier will oscillate at the beginning of the amplification stage but will stabilize over time.

According to the above analysis, different from the structure in Figure 13, the design structure proposed in this study does not need to introduce a compensation capacitance to stabilize the system due to its advantages in structural design, making the design simpler.

The simulation results of the input-referred in-band noise are shown in Figure 21. The sigma value is about −87.29 dB. As the input noise analysis of the cascaded-type FIA and single-stage FIA mentioned earlier shows, the input-referred in-band noise of the structure is similar to that of the structure in Figure 10, indicating that the structure does not need to sacrifice the noise performance of the amplifier when it achieves a high gain, which is also proven by the simulation results. According to the above analysis and actual simulation, the noise performance of the single-stage FIA is better than that of the two-stage FIA. For delta-sigma ADC, we usually only focus on the noise energy in its low frequency passband. Therefore, in order to suppress the flicker noise of the amplifier at low frequency and further improve the noise performance of the integrator [17], the half the sampling frequency chopper switching circuit is introduced to test the circuit as shown in Figure 22. By adding the chopper switching circuit, the flicker noise at the low frequency is moved out of the frequency passband that we care about, thus reducing the in-band noise energy that we care about.

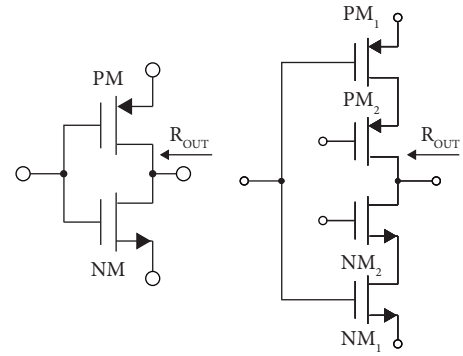

Figure 18: Equivalent output impedance.

The noise of the proposed two-stage dynamic amplifier was tested, and the normal distribution of the input-referred in-band noise was obtained after adding the chopper circuit.

The noise analysis and simulation results obtained after adding chopper switches to different structures when the $C_{RES}s$ are the same are shown in Figures 23–26. The sigma value of the noise after adding the single-stage FIA chopper increases by about 8 dB, and that of the input noise after adding the structure chopper in Figure 10 increases by about 6 dB.

In the cascaded high-gain FIA circuit proposed in this study, one sigma of the input-referred in-band noise after adding the chopper was about −100.26 dB, which increased to about 12 dB. Because of the structural characteristics of the cascaded high-gain FIA proposed in this study, the size of the input MOSFETs of the first-stage amplifier in the actual design is smaller than that of the second-stage amplifier, as shown in Figure 10.

Therefore, the transconductance of the second-stage amplifier designed in this study will be smaller than that

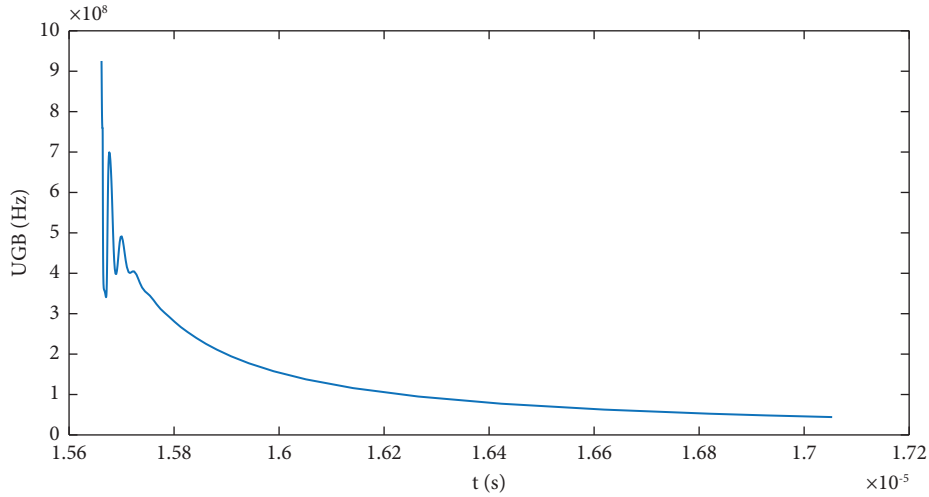

Figure 19: Time varying UBG of the proposed two-stage FIA structure.

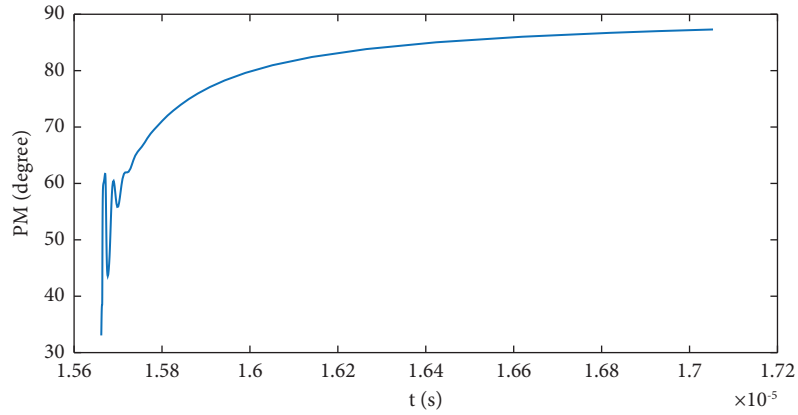

Figure 20: Time varying PM of the proposed two-stage FIA structure.

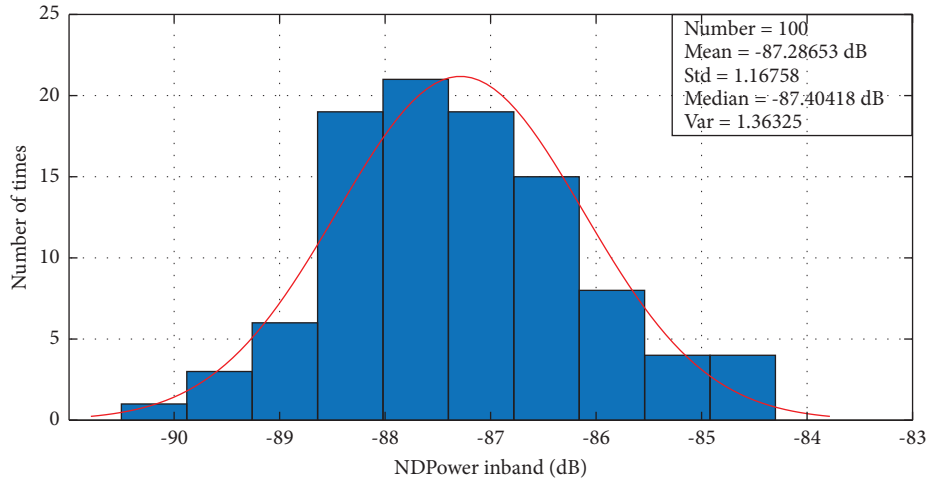

Figure 21: Histogram of the normal distribution of the input noise of the two-stage high-gain FIA.

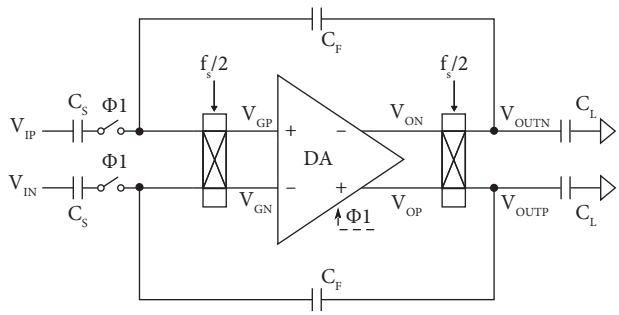

Figure 22: Unity-gain SC integrator with chopper switches.

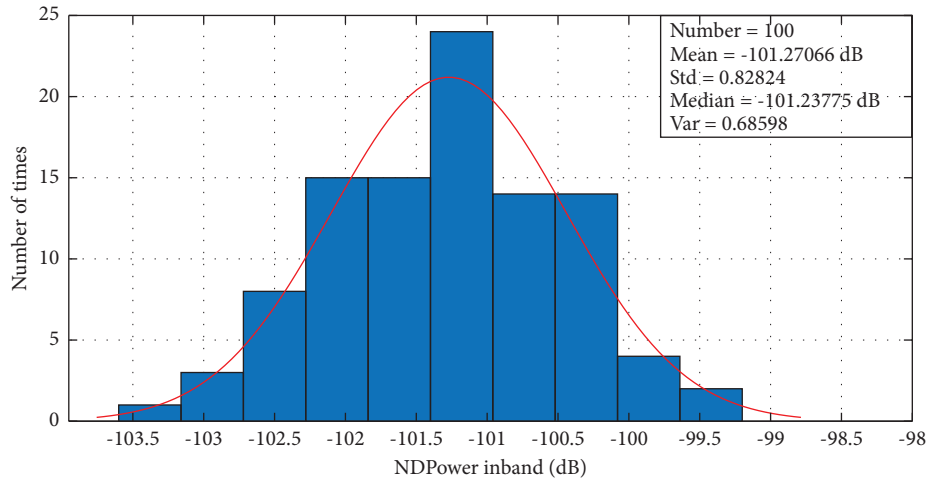

Figure 23: Input noise of the circuit in Figure 1 with a chopper.

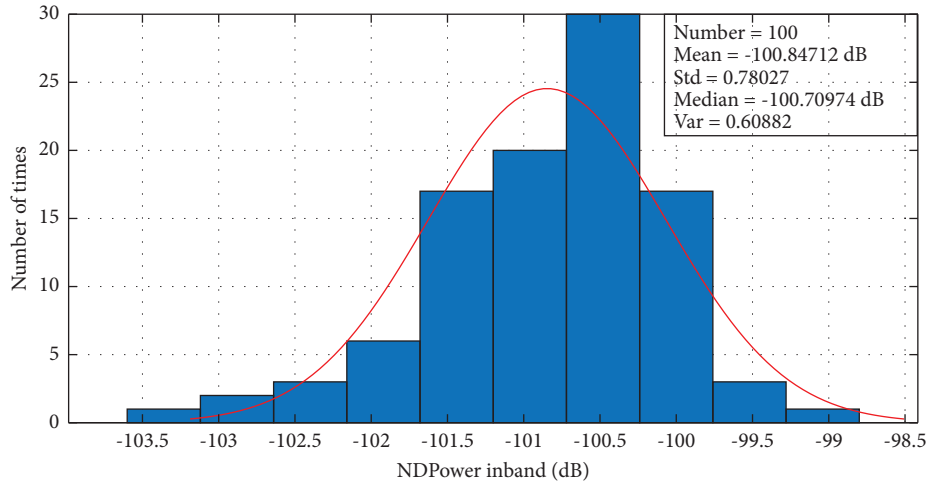

Figure 24: Input noise of the circuit in Figure 6 with a chopper.

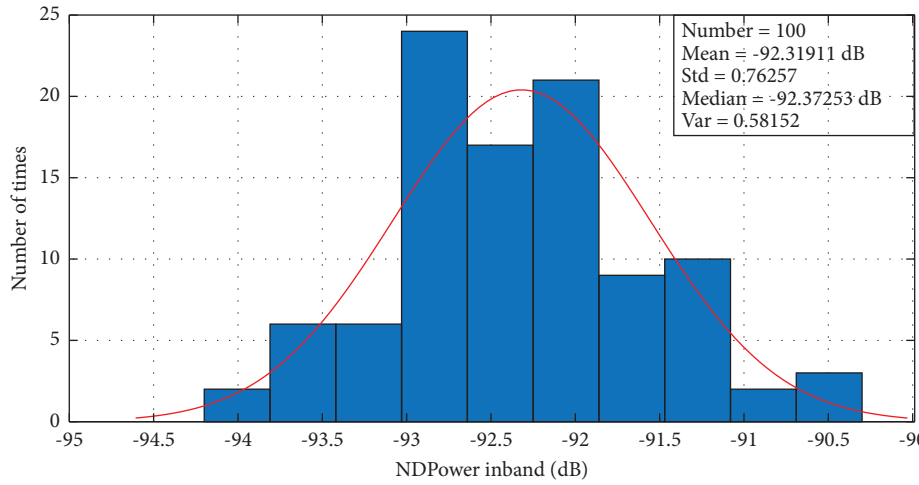

Figure 25: Input noise of the circuit in Figure 10 with a chopper.

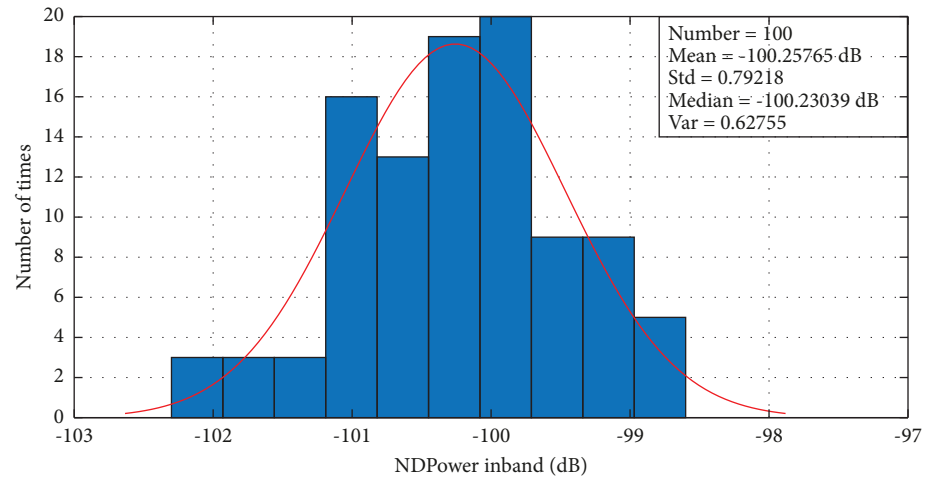

Figure 26: Input noise of the two-stage high-gain FIA with a chopper.

Table 1: FIA structure and performance comparison between the improved amplifiers.

Parameters	Structure			
	FIA [7]	Cascode FIA [9]	INVINV FIA [10]	This work
DC gain	Low	Medium	Medium	High
Output swing	Large	Medium	Large	Medium
In-band noise	Low	Low	Medium	Medium
In-band noise with a chopper	Low	Low	Medium	Low

of the second-stage amplifier of the circuit in Figure 10. According to (2), the noise amplification factor of the structure proposed in this study will be smaller than that of the circuit in Figure 10, so the chopper effect is better than that of the circuit in Figure 10.

5. Conclusion

FIA is an excellent representative of high-energy-efficiency amplifiers in recent years, and ADC innovative designs based on this structure are constantly emerging. However, there is still no relatively perfect basic analysis and research on FIA and its improved structure.

In this paper, the existing FIA structure and its improved amplifier are analyzed and simulated in detail from the aspects of gain, swing, stability, and noise. The results are shown in Table 1. The conclusions are as follows: single-stage FIA is more suitable for low-noise applications, while for high-precision applications with a high input dynamic range, two-stage FIA has obvious advantages of high gain.

It can be seen that the SC integrator using the new amplifier proposed in this paper has a greater closed-loop

DC gain and excellent noise performance and is suitable for the design of delta-sigma ADC with high precision and high input dynamic range. The SC integrator based on the amplifier is designed and verified by the SMIC 180 nm CMOS process under a power supply voltage of 1.2 V.

Data Availability

The data used to support the findings of this study are available from the corresponding author upon request.

Conflicts of Interest

The authors declare that there are no conflicts of interest related to this paper.

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