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Improved Subthreshold Characteristics by Back-Gate Coupling on Ferroelectric ETSOI FETs

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Abstract

In this work, extremely thin silicon-on-insulator field effective transistors (ETSOI FETs) are fabricated with an ultra-thin 3 nm ferroelectric (FE) hafnium zirconium oxides ($Hf_{0.5}Z_{r0.5}O_2$) layer. Furthermore, the subthreshold characteristics of the devices with double gate modulation are investigated extensively. Contributing to the advantages of the back-gate voltage coupling effects, the minimum subthreshold swing (SS) value of a 40 nm ETSOI device could be adjusted from the initial 80.8–50 mV/dec, which shows ultra-steep SS characteristics. To illustrate this electrical character, a simple analytical model based on the transient Miller model is demonstrated. This work shows the feasibility of FE ETSOI FET for ultra-low-power applications with dynamic threshold adjustment.

Keywords: $Hf_{0.5}Zr_{0.5}O_2$, ETSOI, Back gate, Subthreshold swing, Domain switching

Background

To fabricate an ultra-low-power CMOS integrated circuits, many researches have investigated field effect transistors (FETs) with new structures [1–3] or revolutionary principles [4, 5]. Extremely thin silicon-on-insulator (ETSOI) FETs, which have improved the gate control ability and reduced the leakage by the fully depleted channel and bottom isolation, respectively, are proposed to realize ultra-low-power-consumption circuits [6–15]. However, the devices cannot break the limitations of "Boltzmann tyranny" only by structural innovation. Ferroelectric ETSOI FETs (FE ETSOI FET), which integrate a ferroelectric (FE) film into the gate stacks, could realize the amplification of the surface voltage on the channel and achieve super-steep SSs (< 60 mV/dec) [16–18]. In the past several years, the improved subthreshold characteristics of the FE ETSOI FETs were reported [19, 20]. Although the subthreshold characteristics could be improved, there are few works revealing the back-gate coupling effect on the performances of the FE devices.

In this work, ETSOI FETs are fabricated with an ultra-thin 3-nm-thick FE hafnium zirconium oxides ($Hf_{0.5}Zr_{0.5}O_2$) film. Based on the advantages of double gate structure of the devices, a method for improving the subthreshold characteristics of FE ETSOI FETs by back-gate voltage coupling is demonstrated. The values of the subthreshold swing (SS) could be adjusted from 80.8 to 50 mV/dec by the back-gate voltage modulating for a 40 nm physical gate length (L_G) ETSOI device, which shows obvious ultra-steep SS characteristics. To illustrate this electrical character, a simple analytical model based on the transient Miller model is used in this work.

Method

Devices were fabricated on SOI wafers with a buried oxide (BOX) thickness of 145 nm. A process fabrication flow of the ETSOI MOSFET is depicted in Fig. 1a. The ultra-thin top Si layers of the SOI substrates are

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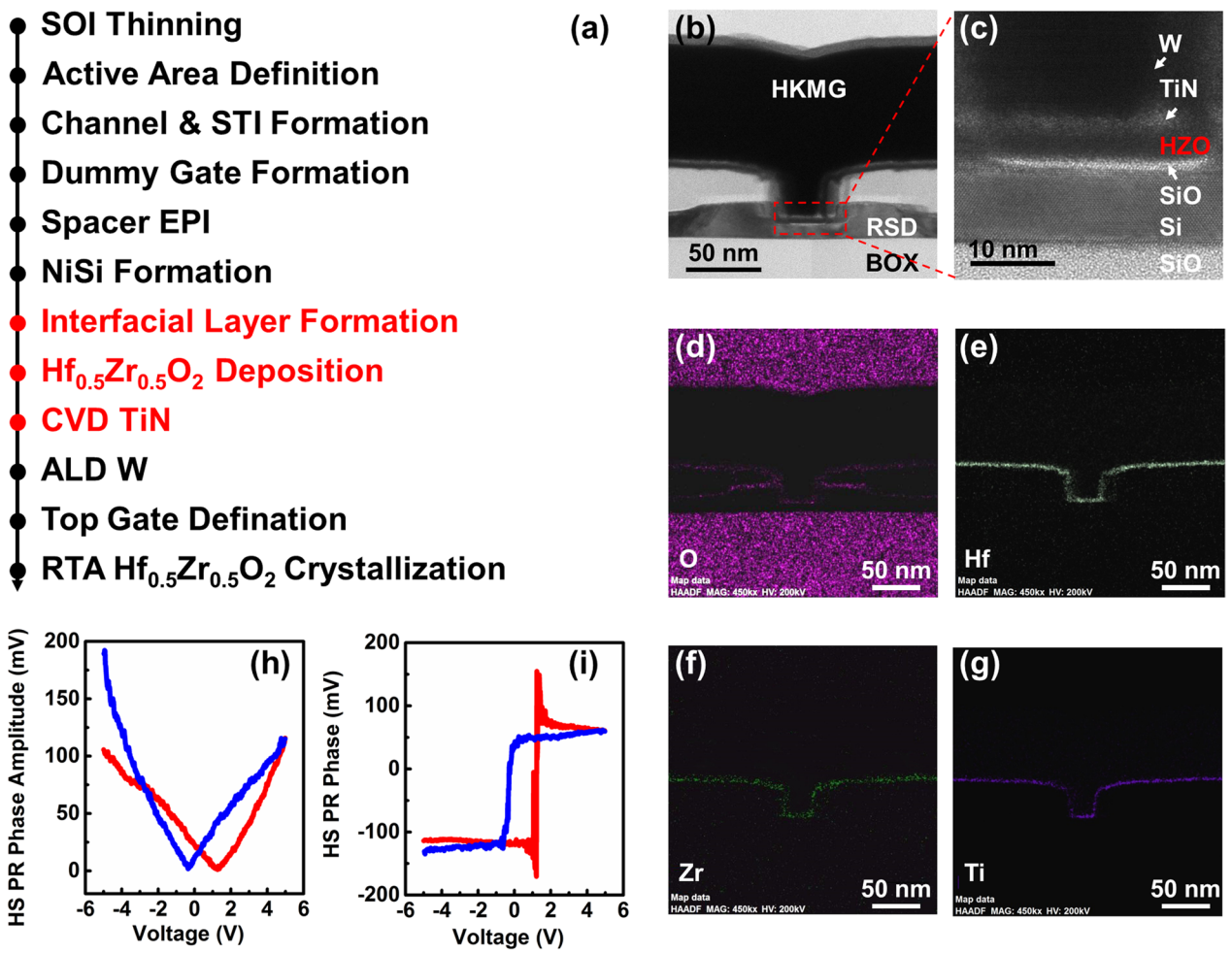

Fig. 1 (**a**) Process flow of $Hf_{0.5}Zr_{0.5}O_2$ ETSOI *n*-type MOSFETs fabrication, (**b**) TEM cross-sectional image for $Hf_{0.5}Zr_{0.5}O_2$ ETSOI MOSFETs with raised source/drain structure and ultra-thin channel, (**c**) enlarged image of the gate stacks in (**b**). (**d**) O, (**e**) Hf, (**f**) Zr and (**g**) Ti elements distribution of the ETSOI MOSFETs. (**h**) PFM phase and (**i**) amplitude hysteresis loops taken on the TiN top electrode with 3 nm $Hf_{0.5}Zr0_{.5}O_2$

thinned to 7 nm by thermal oxidation followed by diluted hydrofluoric acid. Dummy poly gates were formed followed by ultra-thin spacers (~8 nm). Faced raised source and drain (RSD) was epi-grown with in situ doped boron ions. In order to form high-quality raised SiGe SD, the thickness of silicon loss in SD area needs to be carefully controlled. In the flowing steps, an additional implantation of As and a rapid thermal anneal (RTA) process was performed to drive in the doped ions to form the extensions. After self-allied silicide formation, dummy poly gates were removed. In the flowing steps, after the ~ 1 nm SiO2 interfacial layer (IL) formation by chemical O_3 oxidation, a sequential deposition of multilayer $Hf_{0.5}Zr_{0.5}O_2$ and TiN films was performed by an atomic layer deposition (ALD) and chemical vapor deposition (CVD) process, respectively, where the FE $Hf_{0.5}Zr_{0.5}O_2$ material replaced the conventional HfO_2 film. The $Hf_{0.5}Zr_{0.5}O_2$ film (3 nm) was deposited by ALD at 300 °C using Hf (TEMAH) and Zr (TEMAZ)-based organic precursors. A RTA process of 550 °C/30 s at nitrogen atmosphere was carried out after the deposition of $Hf_{0.5}Zr_{0.5}O_2$, which was also helpful to improve the quality of the $Hf_{0.5}Zr_{0.5}O_2$ film. The SD metal contact by the W-plug and the alloy processes by forming gas annealing (FGA) at 450 °C/30 min were carried out in the subsequent steps. The cross-sectional profiles of FE ETSOI FET were observed using a cross-sectional transmission electron microscope (TEM). The electrical characterization was performed using Keithley 4200 and Agilent 4156C semiconductor parameter analyzers.

Result and Discussion

Figure 1b shows the cross-sectional TEM image of a 40-nm L_G device. High-κ metal gates (HKMGs) multilayers, W/3-nm TiN/3-nm HZO/1-nm SiO (IL), are shown in Fig. 1c. In this figure, multilayer HKMGs distributed on the channel are highly conformal and uniform. The thicknesses of the IL and FE layers, labeled in Fig. 1c, are about 1 nm and 3 nm, respectively, and the ultra-thin Si channel layer is 7 nm in thickness, which contributes to better control of the short channel effects (SCEs) than that of bulk MOSFET. Figure 1d–g show the elements distribution of the FE device. It can be seen that Hf and Zr atoms are basically concentrated in the medium layer, and there is no diffusion for multilayer materials. The above results show that the process controls appropriate during manufacturing process of the device, and the $Hf_{0.5}Zr_{0.5}O_2$ has good process compatibility with the conventional CMOS fabrication.

Furthermore, to confirm the ferroelectricity of the HZO film, capacitors with TiN /3-nm HZO/ ~ 1-nm SiO_2/Si were fabricated, which own similarly conditions with the devices, and analyzed by piezoresponse force microscopy (PFM) test using Asylum MFP-3D. Figure 1h and i show corresponding results for the characterization with a typical frequency range ~ 350–400 kHz. The presence of square 180° hysteresis in PFM phase indicates the upward and downward polarization states, and butterfly-shaped loops in PFM amplitude implies robust remanent polarization for the FE film.

Figure 2a shows the transfer curves (I_{DS}–V_{GS}) of a 40-nm L_G FE ETSOI FETs at V_{DS}s of 50 and 900 mV, respectively. The calculated value of the drain-induced barrier lowering (DIBL) is ~ 130 mV/V indicating serious SCEs. In addition, Fig. 2b summarizes the corresponding variations of SSs as a function of V_{GS} for the devices. The results show that the minimum value of the SS is higher than 82 mV/dec, which is much higher the limit value of "Boltzmann tyranny."

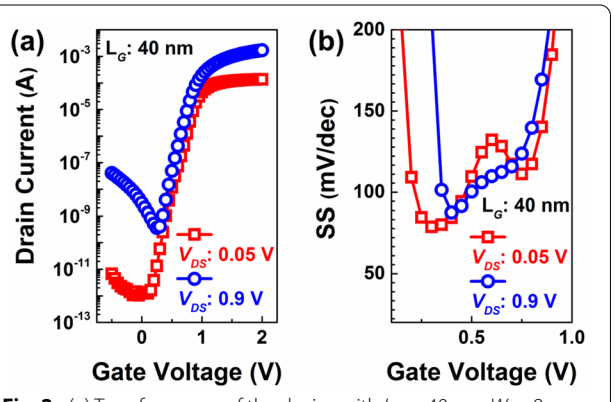

Fig. 2 (**a**) Transfer curves of the device with $L_G = 40$ nm, $W = 8$ μm. (**b**) Extracted SSs as a function of the V_{GS} of the device

In order to improve the SCEs, based on the advantages of double gate structure of the devices, a method for enhancing the subthreshold characteristics by back-gate voltage coupling effects is demonstrated and analyzed, subsequently. The I_{DS}–V_{GS} of a 40-nm L_G device at $V_{DS} = 50$ mV ($V_{DS@LIN}$) and 900 mV ($V_{DS@SAT}$) with various bias gate voltages (V_{SUB}) from −35 to 35 V are shown in Fig. 3a and b, respectively. When the value of V_{SUB} bias is positive, there is an obvious shoulder near $I_{DS} = 10^{-8}$ A. But when the value of V_{SUB} bias is changed to negative, the shoulder disappears. This indicates that the back channel of the device has a parasitic device which is also controlled by V_{GS}. The positive bias will enhance the parasitic effect, while the negative bias can turn off the parasitic effect.

Figure 3c summarizes the corresponding variations of threshold voltage (V_Ts) and factors of DIBLs as a function of V_{SUB}s for the device shown in Fig. 3a. All of the corresponding V_T values are extracted at a fixed normalized I_{DS} of 10 nA/μm. It can be seen that both $V_{T@LIN}$ and $V_{T@SAT}$ increase linearly with V_{SUB} changing from positive to negative. With different bias of the V_{SUB}, the V_T can be tuned within the range of almost 1.5 V. It demonstrates V_{SUB} bias can be effectively served as a method to modulate ETSOI device characteristics due to the controlling of carrier confinement. Furthermore, it is worth noting that with the decrease of V_{SUB}, the difference between $V_{T@LIN}$ and $V_{T@SAT}$ tends to decrease gradually, which means smaller values of the DIBLs and the improved SCEs.

With V_{SUB} value decreasing continuously, the value of $V_{T@LIN}$—$V_{T@SAT}$ shows a decrease tendency and changed from positive under + V_{SUB} to negative under some -V_{SUB} value, which indicates the phenomenon of the negative DIBL (N-DIBL). With various V_{SUB} bias, the behaviors of SCEs are different. For positive V_{SUB} bias, currieries were pulled away from top channel, and thus, DIBL gets worse. Besides, for negative V_{SUB} bias, top gate controllability of channel carriers was enhanced, thereby achieving better DIBL performance. Furthermore, the random variation of DIBLs, especially for those negative DIBLs, may be caused by the transit negative capacitance phenomenon induced by the HZO film in the gate stacks [21]. In addition, Fig. 3d summarizes the corresponding variations of SSs as a function of V_{DS} for the devices. Corresponding to the above results, with the decrease of V_{SUB}, the values of SSs show a decreasing trend and the minimum SS value of the device reaches 50 mV/dec at $V_{DS} = 50$ mV and $V_{SUB} = -35$ V, which is far below the limit of 60 mV/dec for the conventional FETs and exhibiting the great advantage for ultra-low-power application. Due to the shoulder

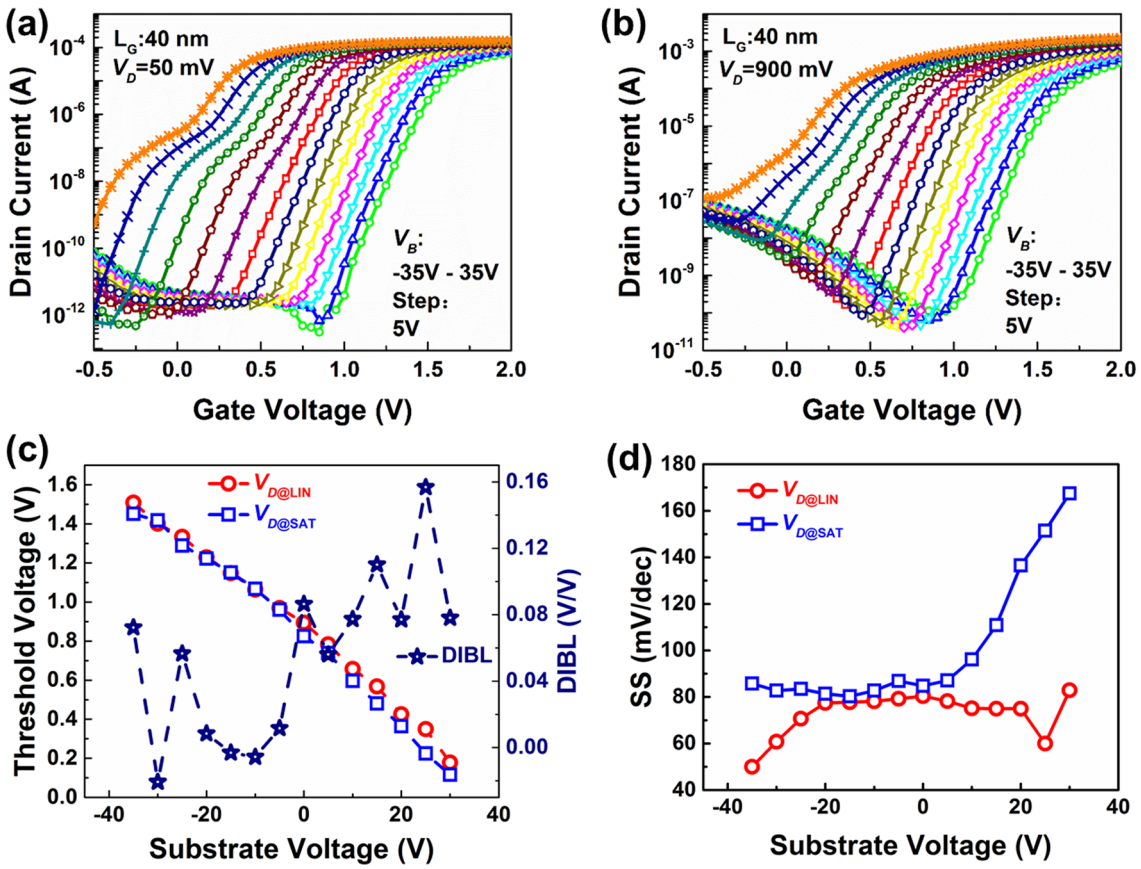

Fig. 3 Impacts of back bias voltages on transfer curves of FE ETSOI FET, with (**a**) $V_{DS} = 0.05$V, and (**b**) $V_{DS} = 0.9$ V, with $L_G = 40$ nm. (**c**) Extracted V_Ts and DIBLs under various V_{SUB}s of the device in Fig. 3a. (**d**) Extracted SSs under various V_{SUB}s of the device in Fig. 3a and (b).

existing under high positive V_{SUB} with 50 mV V_D, the accurate minimum SS values should be higher than that shown in Fig. 3d, but it does not affect the conclusion that subthreshold characteristics improving under negative V_{SUB}.

To illustrate the mechanism of the substrate voltage enhancing SCEs of FE ETSOI FET, a simple analytical model based on ferroelectric domain switching is used shown in Fig. 4. Figure 4a shows capacitance coupling in fabricated FE ETSOI FET, where C_{FE}, C_{DE}, C_{CHAN} and C_{BOX} are capacitance of FE film, silicon oxide dielectric layer, silicon channel and box silicon oxide, respectively. C_{MOS} can be written as $(C_{MOS}{}^{-1} = C_{DE}{}^{-1} + C_{CHAN}{}^{-1} + C_{BOX}{}^{-1})$. According to the transient Miller model [22, 23], the equivalent circuit model of this DE–FE network is shown in Fig. 4b. Considering current flowing through the FE–DE stack, the equation for V_{RFE} as $V_{RFE} = R_{FE} \times I = (\tau/C_{FE}) \times I = (\tau/C_{FE}) \times C_{FE} \quad (dV_{CFE}/dt) = \tau \times (dV_{CFE}/dt)$ and $V_{RFE} = [\tau \times C_{DE}/(C_{DE} + C_{FE})] \times [dV_{GS}/dt - dV_{FE}/dt + dV_{CFE}/dt]$ can be written. Here, V_{FE} and V_{RFE} are voltage drops across C_{FE} and R_{FE}, and τ is the lag between V_{FE} and the polarization (P). After differentiating these two equations with respect to time (t), an equation for dV_{FE}/dt can be derived. For ultra-steep SS characteristics, dV_{FE}/dt should change from a positive to a negative value in case of positive ramp (dV_{GS}/dt and dP/dt are positive) or negative to positive for negative ramp. Therefore, the condition for ultra-steep SS characteristics in the DE–FE network can be written as the following equation:

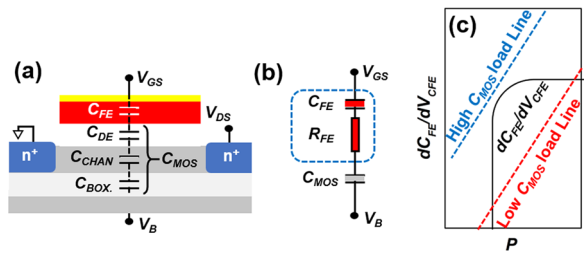

Fig. 4 (**a**) Capacitance in FE ETSOI MOSFET. (**b**) Equivalent circuit model of DE–FE network according to Miller model. (**c**) Graphical representation of the equation with respect to P for different values of C_{MOS}.

$$\left|\frac{dC_{FE}}{dV_{CFE}}\right| > \left[1-\frac{d\tau}{dt}\right]\left[\frac{\tau}{CMOS+CFE}\left|\frac{dV_{GS}}{dt}\right| * \left|\frac{dC_{FE}}{dt}\right|\left(\frac{dV_{CFE}}{dV_{GS}}\right)\right]^{-1}$$

This equation suggests that the increase in C_{FE} with V_{CFE} is the prime factor for the ultra-steep SS characteristics, which must be sufficiently large. The discussion in this work assumes that τ, dC_{FE}/dt and dV_{CFE}/dV_{GS} are not affected by V_{SUB} changing, so we can conclude from the equation that ultra-steep SS will be easier to meet with decrease in C_{MOS}.

For the fabricated FE ETSOI MOSFET, as V_{SUB} increases, the energy band of the channel gradually bends, that is to say, more electrons could fill the channel. Due to the charge shielding effects of the filled electrons, the C_{MOS} value gradually increases. As Fig. 4c shown, with a low C_{MOS} value, the inequality is easier to establish, and thus, the ultra-steep SSs are more easily to be obtained [22].

Conclusion

In this work, an innovative way to enhance the subthreshold characteristics effects by coupling back-gate voltage is proposed and realized initially with FE ETSOI MOSFETs. The minimum SS value of a 40 nm ETSOI device could be adjusted from the initial 80.8 to 50 mV/dec, which shows ultra-steep SS characteristics. A simple analytical model based on the transient Miller model is used in this work to illustrate the mechanism. This work demonstrates the feasibility of FE ETSOI MOSFET in ultra-low-power application with dynamic threshold adjustment.

Abbreviations

ETSOI FETs: Extremely thin silicon-on-insulator field effective transistors; FE: Ferroelectric; $Hf_{0.5}Zr_{0.5}O_2$: Hafnium zirconium oxides; SS: Subthreshold swing; IL: Interfacial layer; ALD: Atomic layer deposition; CVD: Chemical vapor deposition; TEM: Transmission electron microscope; L_G: Gate length; HKMGs: High-κ metal gates; SCEs: Short channel effects; PFM: Piezoresponse force microscopy; I_{DS}–V_{GS}: Transfer curves; DIBL: Drain-induced barrier lowering; N-DIBL: Negative DIBL.

Author Contributions

ZZ and YL wrote the main manuscript text. JX, BT, JX, JL and QZ prepared the devices. ZW, HY, JL and WW supervised the project and discussed the questions in this work. All authors read and approved the final manuscript.

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Availability of Data and Material

The datasets supporting the conclusions of this article are included in the article.

Declarations

Ethics Approval and Consent to Participate

Not applicable.

Consent for Publication

Not applicable.

Competing interests

The authors declare that they have no competing interests.

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References

1. Krivokapic Z, Rana U (2017) 14nm ferroelectric FinFET technology with steep subthreshold swing for ultra-low power applications. In: IEDM Tech. Dig 15.1.1–15.1.4
2. Zhang Q, Yin H (2021) Optimization of structure and electrical characteristics for four-layer vertically-stacked horizontal gate-all-around Si nanosheets devices. Nanomaterials 11:646
3. Zhang Z-H, Xu G (2019) FinFET with improved subthreshold swing and drain current using 3 nm FE Hf0.5Zr0.5O2. IEEE Electron Device Lett 40:367–370
4. Salahuddin S, Datta S (2008) Use of negative capacitance to provide voltage amplification for low power nanoscale devices. Nano Lett 8:405–410
5. Li K-S, Chen P-G (2015) Sub-60mV-swing negative-capacitance FinFET without hysteresis. In: IEDM Tech. Dig 22.6.1–22.6.4
6. Hoentschel J, Pirro L (2019) Technologies for ultra-low power IoT, RF and mmWave Applications. Nanoelectronic Devices 2
7. Weber O, Josse E (2014) 14nm FDSOI technology for high speed and energy efficient applications. Symposium on VLSI Technology 1–2
8. Magarshack P, Flatresse P (2013) A process/design symbiosis for breakthrough energy-efficiency. In: Design, Automation & Test in Europe Conference & Exhibition (DATE) 952–957
9. Colinge JP (2004) Silicon-on-insulator technology: materials to VLSI[M]. Springer, US
10. Cheng K, Khakifirooz A, Loubet N et al (2012) High performance extremely thin SOI (ETSOI) hybrid CMOS with Si channel NFET and strained SiGe channel PFET. In: Proc IEEE IEDM, Dec, pp 419–422
11. Ohata A, Bae Y, Fenouillet-Beranger C et al (2012) Mobility enhancement by back-gate biasing in ultrathin SOI MOSFETs with thin BOX. IEEE Electron Device Lett 33(3):348–350
12. Cavalcante C et al (2020) 28nm FDSOI CMOS technology (FEOL and BEOL) thermal stability for 3D sequential integration: yield and reliability analysis. In: IEEE Symposium on VLSI Technology, pp 1–2
13. Majumdar A, Ren Z, Koester SJ, Haensch W (2009) Undoped-body extremely thin SOI MOSFETs with back gates. IEEE Trans Electron Dev 56(10):2270–2276
14. Bosch D et al (2019) Novel fine-grain back-bias assist techniques for 14nm FDSOI Top-Tier SRAMs integrated in 3D-Monolithic. In: Proc Symp VLSIT, pp 1–2
15. Liu Q, Monsieur F, Kumar A et al (2011) Impact of back bias on ultrathin body and BOX (UTBB) devices. In: Proc Symp VLSIT, Jun, pp 160–161
16. Fenouillet-Beranger C, Thomas O (2010) Efficient multi-V T FDSOI technology with UTBOX for low power circuit design. In: Symposium on VLSI Technology, pp 65–66

17. Vitale SA, Wyatt PW (2010) FDSOI process technology for subthreshold-operation ultralow-power electronics. In: Proceedings of the IEEE
18. Tang Z, Tang B (2014) Impacts of back gate bias stressing on device characteristics for extremely thin SoI (ETSoI) MOSFETs. IEEE Electron Dev Lett 35:303–305
19. Kwon D (2018) Improved subthreshold swing and short channel effect in FDSOI n-channel negative capacitance field effect transistors. IEEE Electron Dev Lett 39:300–303
20. Kwon D (2019) Negative capacitance FET With 1.8-nm-thick Zr-doped HfO_2 Oxide. IEEE Electron Dev Lett 40:993–996
21. Zhou J, Han G (2018) Negative Differential resistance in negative capacitance FETs'. IEEE Electron Dev Lett 39:622–625
22. Saha AK, Datta S (2018) Negative capacitance" in resistor-ferroelectric and ferroelectric-dielectric networks: apparent or intrinsic'. J Appl Phys 123(10):105102
23. Cao W, Banerjee K (2020) Is negative capacitance FET a steep-slope logic switch? Nat Commun 11:1

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