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A 60%-Efficiency 20nW–500μW Tri-Output Fully Integrated Power Management Unit with Environmental Adaptation and Load-Proportional Biasing for IoT Systems

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As Internet-of-Things (IoT) systems proliferate there is a greater demand for small and efficient power management units. Fully-integrated switched-capacitor (SC) DC-DC converters are promising candidates due to their small form factor and low quiescent power, aided by dynamic activity scaling [1–3]. However, they offer a limited number of conversion ratios, making it challenging to use in actual systems since they often require multiple output voltages (to reduce power consumption) and use various input power sources (to maximize flexibility). In addition, maintaining both high efficiency and fast load response is difficult at low output current levels, which is critical for IoT devices as they often target low standby power to preserve battery charge. This paper presents a fully integrated power management system that converts an input voltage within a 0.9V–5V range to 3 fixed output voltages – 0.6V, 1.2V, and 3.3V. A 7-stage binary-reconfigurable DC-DC converter [2] enables the wide input voltage range. Three-way dynamic frequency control maintains converter operation at near-optimum conversion efficiency under widely varying load conditions from 5nW to 500μW. A proposed *load-proportional* bias scheme helps maintain high efficiency at low output power, fast response time at high output power and retains stability across the entire operating range. Analog drop detectors improve load response time even at low output power, allowing the converter to avoid the need for external sleep/wakeup control signals. Within a range of 1V–5V input voltage and 20nW–500μW output power, the converter shows >60% conversion efficiency while maintaining responsiveness to 100X sudden current increase.

Figure 8.5.1 explains the overall structure of the full system (top) and its operation (bottom). It contains three SC converters (binary-reconfigurable SC up/downconverter, 1:3 Dickson upconverter, 2:1 SC downconverter) with each responsible for generating one of the three output voltage: 1.2V, 3.3V, and 0.6V. The binary-reconfigurable up/downconverter converts a wide range of input voltage into a 1.2V output voltage. The Dickson upconverter and 2:1 downconverter then receive this 1.2V output and convert it into 3.3V and 0.6V, respectively. Proper conversion ratio configuration of the binary converter is important for robust and power-efficient 1.2V generation. If the ratio is set too low, the binary converter output cannot reach 1.2V while if the ratio is set too high, conversion efficiency worsens due to large conduction loss. The system regulates the conversion ratio by using both feedback and

feedforward control [3]. When the system input voltage (V_{BAT}) becomes available, the main controller starts up and turns on the binary converter with a small default ratio. Conversion ratio is continually increased by feedback control until the converter output voltage V1P2 reaches ~1.2V, which triggers the 'output on detector'.

At this point, the 1:3 Dickson upconverter turns on and generates the higher voltages 2.4V and 3.3V. The 2.4V is then used to power an internal 1.2V voltage reference and LDO to generate a clean reference voltage V_{REF} for more accurate regulation of the 1.2V supply voltage. After V_{REF} becomes available, feedforward control acts to set the binary conversion ratio by directly computing the desired conversion ratio using a 8-bit ADC. After the ADC has measured the battery voltage, the conversion ratio is calculated in digital logic to be the measured ratio V_{REF} / V_{BAT} plus an offset value; this allows for an optimal voltage drop to balance conduction and switching losses, maximizing efficiency. After the system is fully turned on, the binary converter ratio is periodically adjusted while supplying output voltages, allowing for self-adaptation in the face of slow input voltage drift arising from battery discharge or temperature changes, both of which frequently occur in wireless IoT systems.

Figure 8.5.2 shows the structure of the three SC converters: a 7-bit binary-reconfigurable up/downconverter, a 2:1 SC downconverter, and a 1:3 Dickson upconverter. The 7-bit binary converter (Fig. 8.5.2, top) consists of seven 2:1 SC converters with configuration switches following a recursive topology [2]. Because the supply voltage level into each stage varies dynamically as the conversion ratio is continuously reconfigured, flying capacitance drivers are implemented by level shifters using cross-coupled PMOS and NMOS switches to maintain the same clock swing and current drivability regardless of their voltage levels. Whenever the conversion ratio changes the intermediate voltages among stages have to be refreshed, while each internal node in the cross-coupled switches must be stabilized with respect to its corresponding intermediate voltage. This yields a chicken and egg problem because intermediate voltages can be stabilized into new values only when the cross-coupled switches are working properly, however these switches work properly only when the intermediate voltages are stabilized. By alternating normal operation and reset of the SC converters by a periodic reset generator (Fig. 8.5.2, bottom left), those two floating nodes can be stabilized at the same time when necessary.

In addition to conversion ratio adjustment, DC-DC converters in IoT systems should be able to self-adapt to widely varying output load conditions to maintain good efficiency. Fig. 8.5.3 shows the frequency control loop of the binary converter, consisting of a main feedback path and a fast voltage drop detection path. For initial startup, the main path compares the first stage output *V1* with the divided input voltage, maintaining a proper amount of voltage drop Δ through the first stage for optimum conversion efficiency. After the system is fully turned on, the binary converter output V1P2 is compared to V_{REF} to be the same level as V_{REF}. Given this ability to maintain a constant output voltage level, the binary converter offers near-optimum efficiency across load conditions as the conversion ratio is already configured for a proper voltage drop amount for optimum efficiency (via the feedforward ratio control path). The 1:3 Dickson upconverter and 2:1 downconverter also have similar frequency control loops for their own oscillators, allowing each of the 3 converters to independently adapt to different load currents at their corresponding output voltages.

The entire control loop operates with a divided converter clock to maintain dynamic power consumption that is proportional to the SC converter switching loss. This ensures that efficiency loss due to the control loop is always a small predictable value regardless of load current level. Other digital blocks are also clocked by this divided converter clock (Fig. 8.5.3, bottom right). This helps reduce their power consumption relative to the system's output power level, but also maintains control loop stability since the operating speed of the various blocks are all scaled by the same factor – hence, blocks can communicate with each other at similar relative response speed, including voltage output.

While the load-proportional speed adjustment scheme offers these benefits, it also has a drawback in the case of small output power. In that case the system responds slower relative to external condition changes such as a sudden load current increase. To address this problem, the frequency control loop in each converter has a dedicated fast voltage drop detector that monitors converter output voltage and triggers a drop detection signal when it goes below certain threshold. The drop detector requires periodic reset to detect output voltage change and maintain a certain threshold level. Hence each converter contains two drop detectors for uninterrupted overlapping operation and detection: one detector always remains on while the other is being reset. By focusing only on triggering upon a fast single drop event without considering stability or continuous operation, the detector's response time can be boosted hundreds times faster (simulation) than the main feedback path, rendering the control loop fast enough for sudden current load changes. Once the detection signal is triggered, the clock frequency is set to its maximum, quickly restoring the output voltage to safe levels. Afterwards, feedback through the main path slowly lowers the clock frequency to support any sustained increase in load current. Drop detector bias current is also adjusted to be load proportional.

The power management system chip was fabricated in 0.18um CMOS and a die photo is shown in Figure 8.5.7. As shown in Figure 8.5.4, the system stably delivers 1.2V, 3.3V, and 0.6V output voltages from an input voltage ranging from 0.9V to 5V. Figure 8.5.5 (top) shows the drop detector responds to 100X sudden load current increase. Graphs at the bottom shows the converter supplies 20nW – 500μ W with >60% efficiency. Figure 8.5.6 summarizes result and compares the design with previous relevant work.

References

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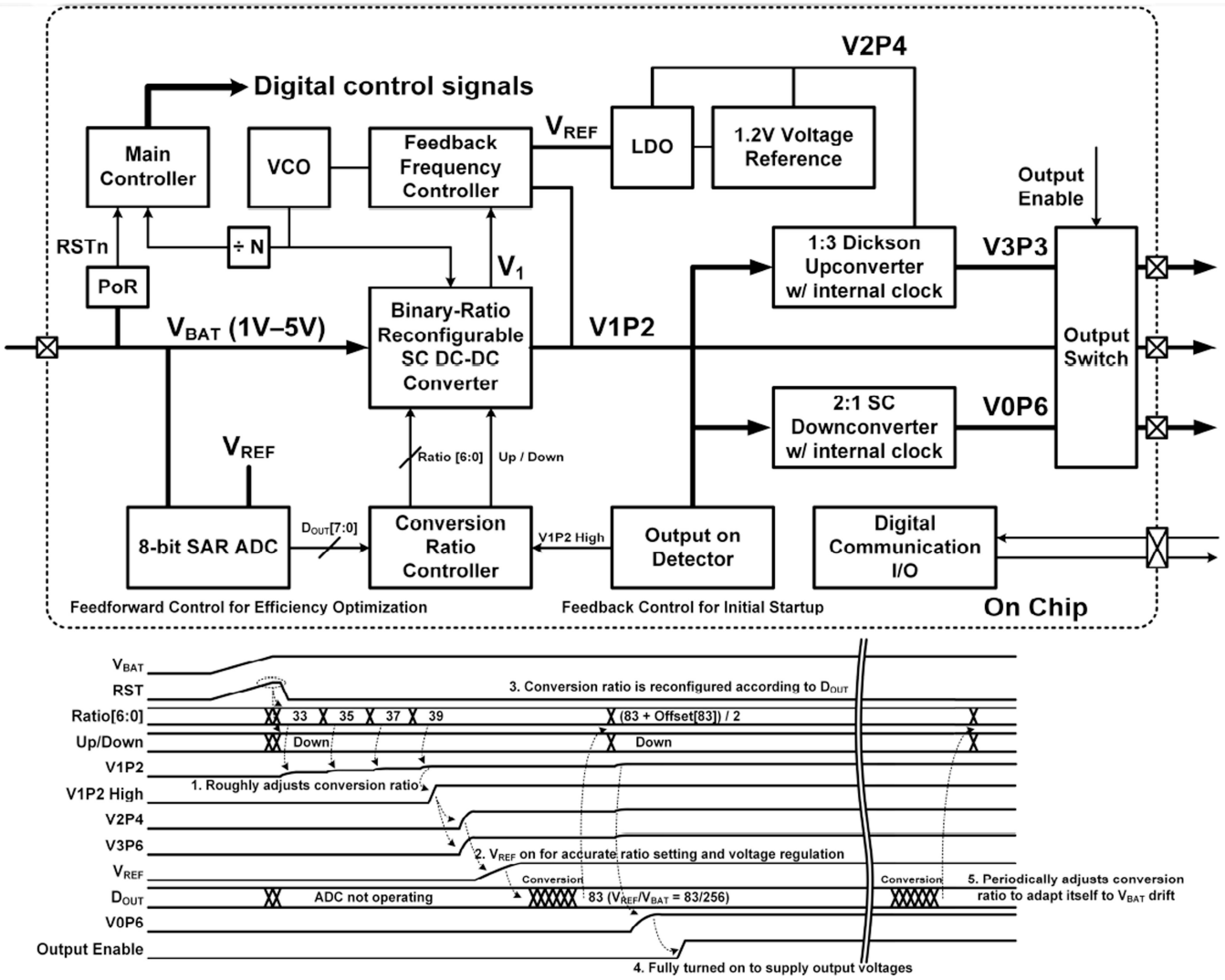

Figure 8.5.1.
Overall architecture of the complete power-management system and its operation.

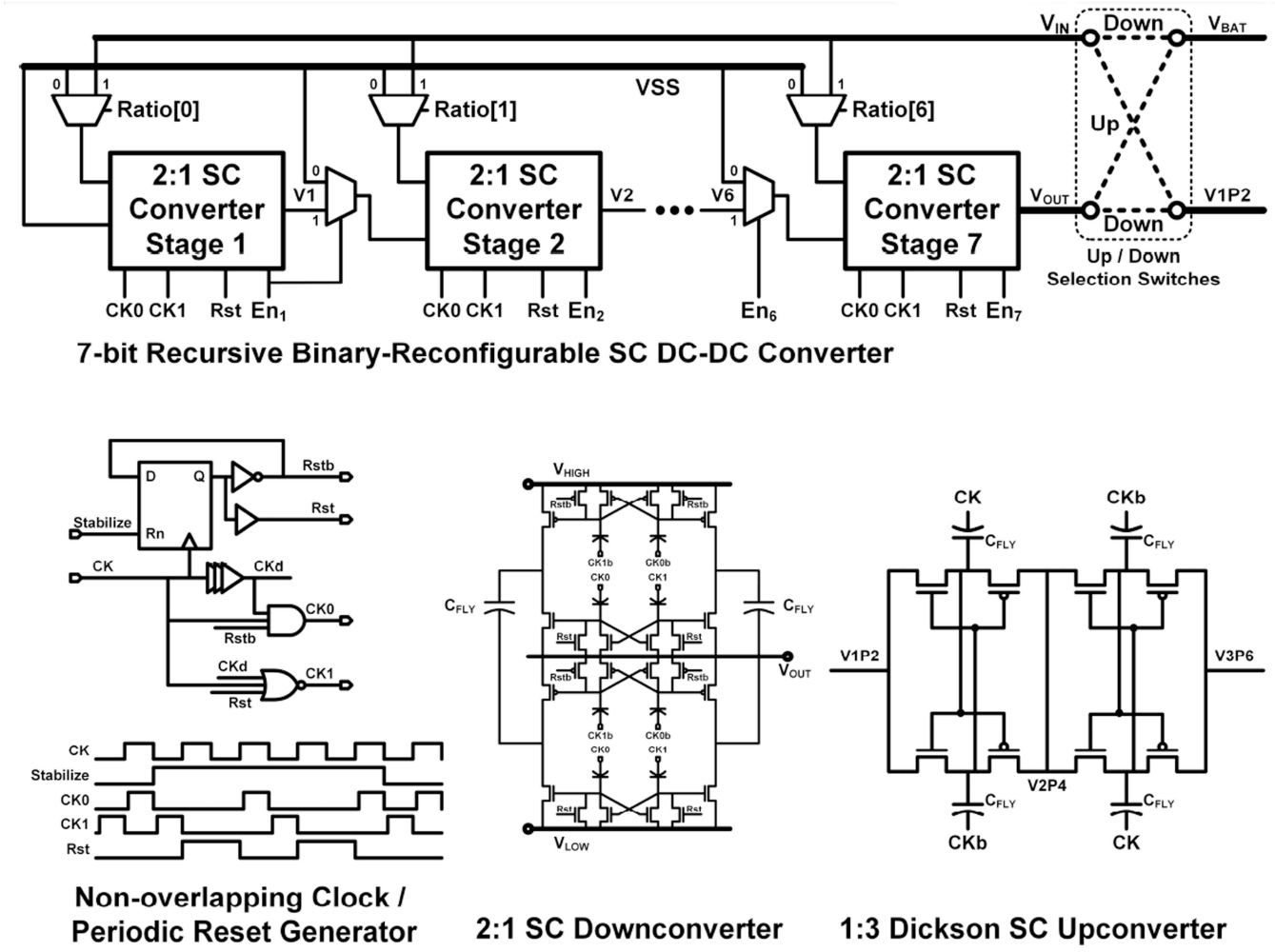

Figure 8.5.2.
Structure of SC converters.

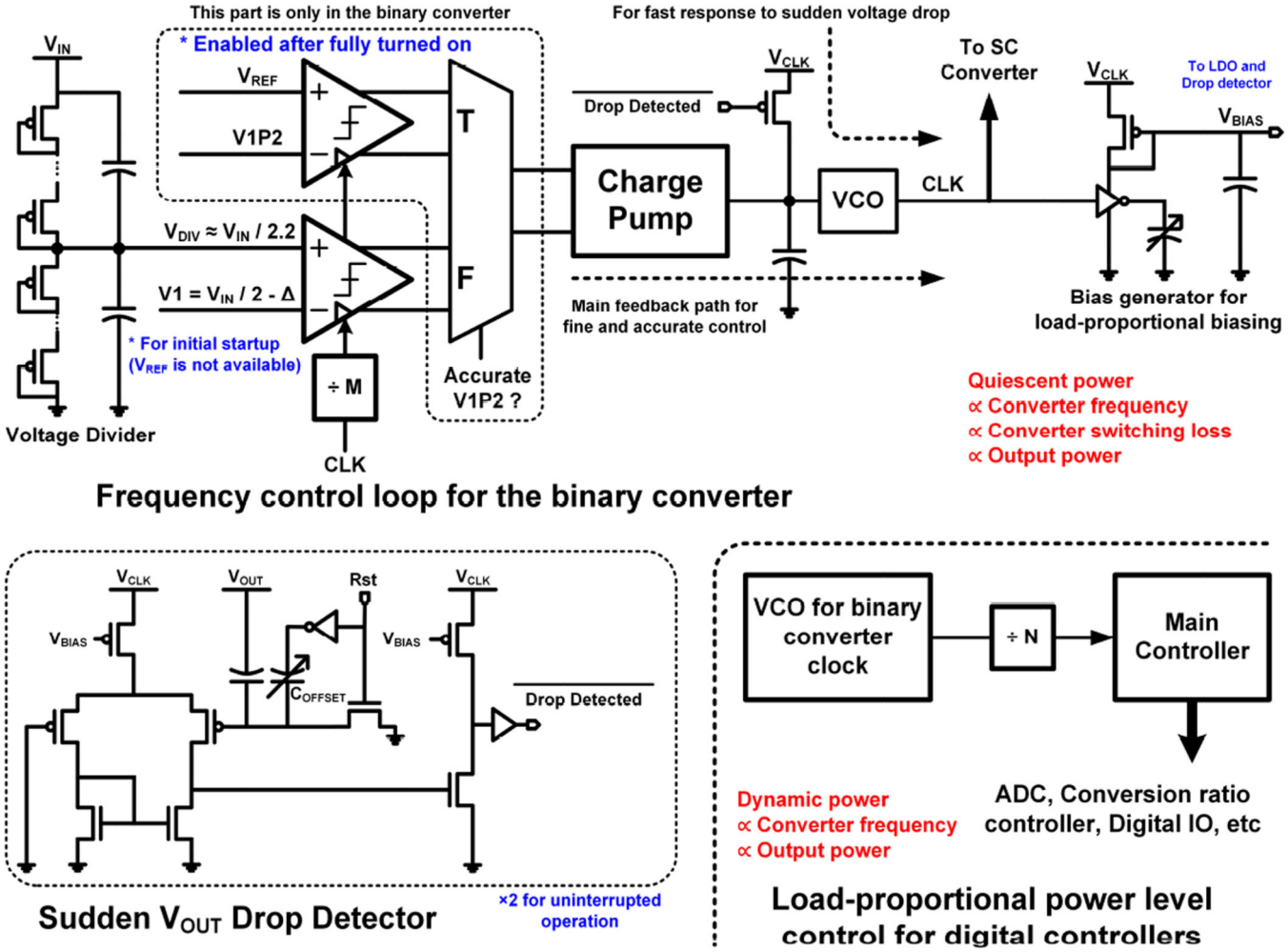

Figure 8.5.3.
Frequency control loop with load-proportional biasing scheme.

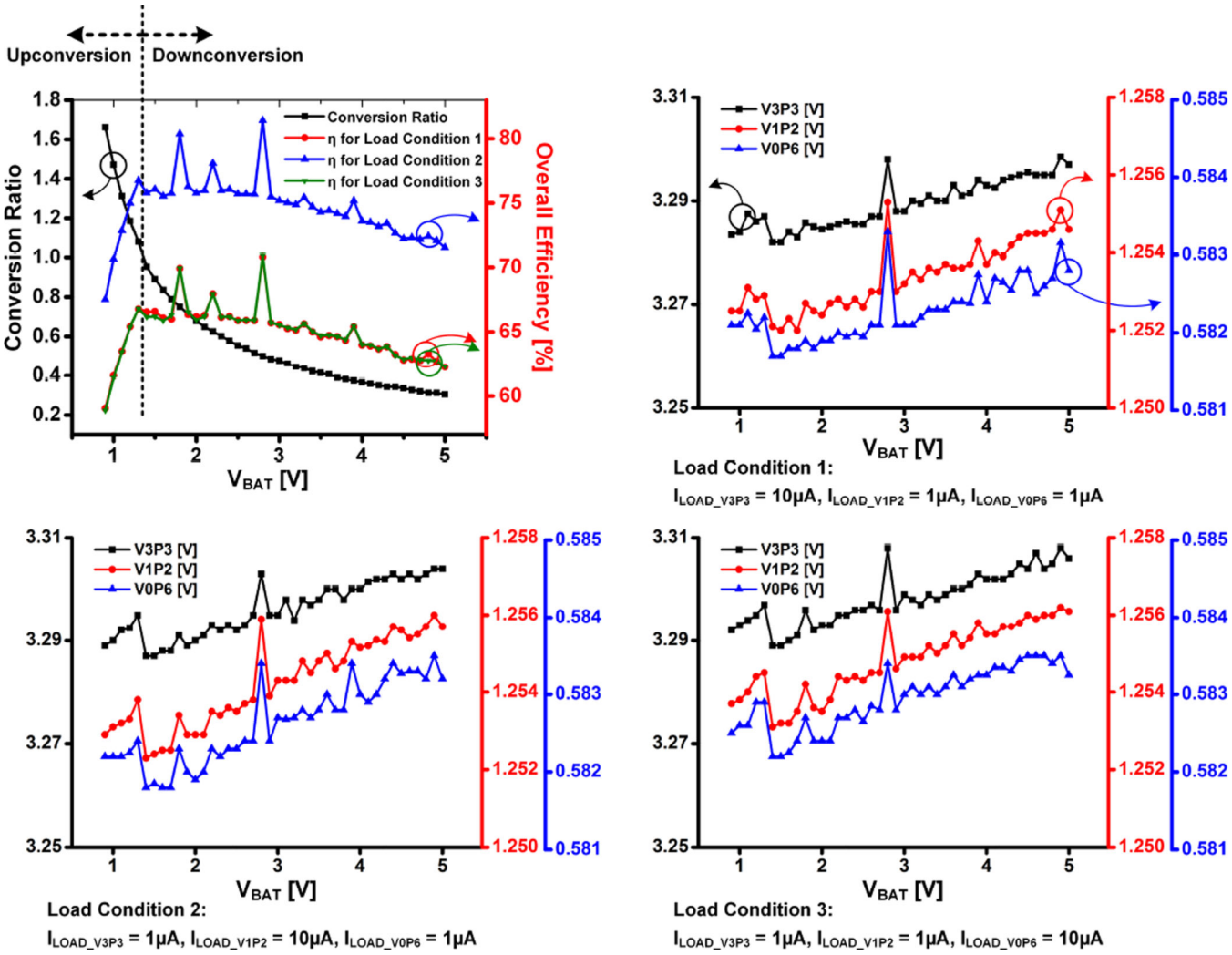

Figure 8.5.4.
Measured performance vs. input voltage.

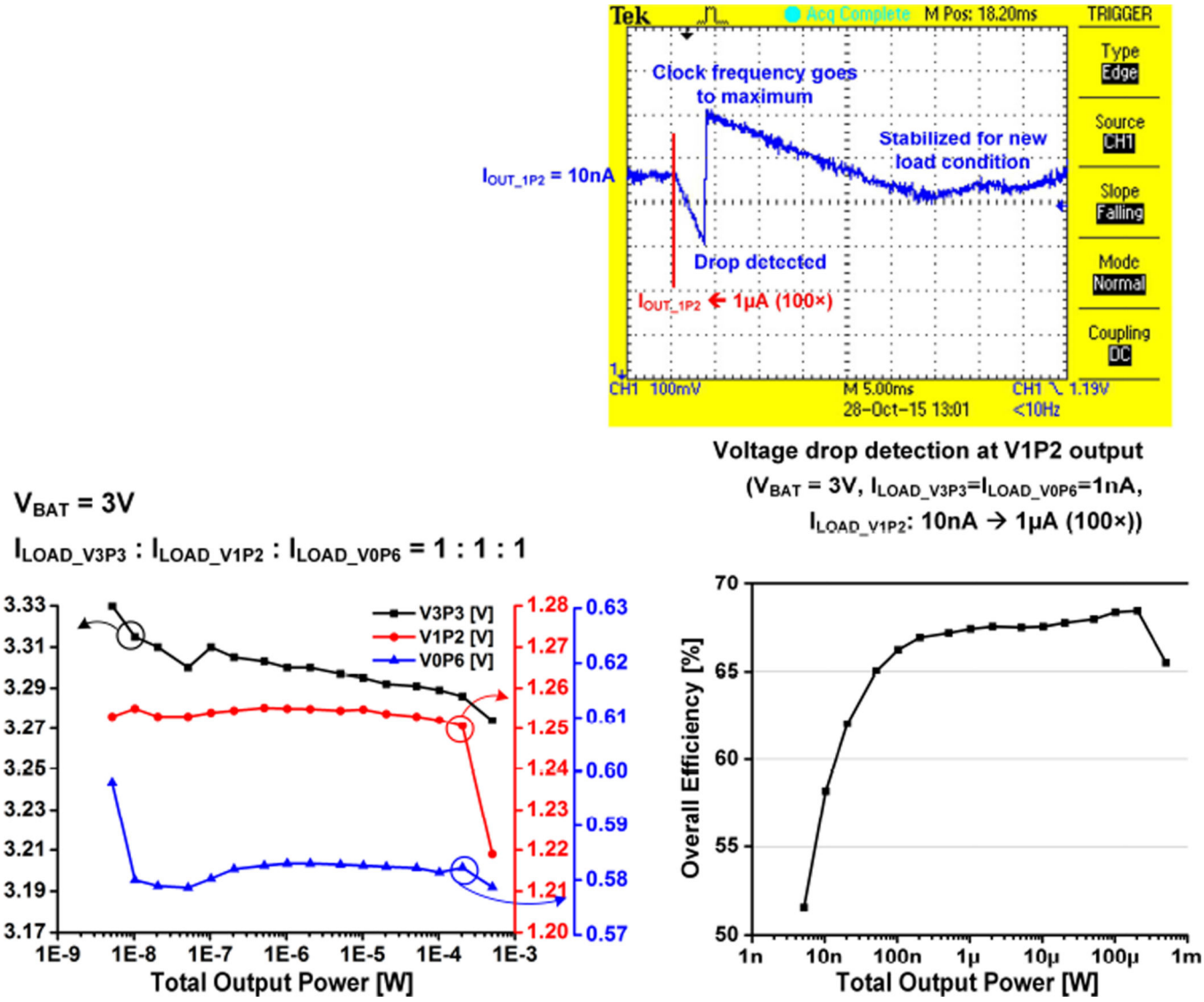

Figure 8.5.5.
Measured drop detector operation (top) and performance vs. output power (bottom).

Metric	[1]	[2]	[3]	This Work
Topology	7-b SAR SC	4-b Recursive SC	Series-Parallel SC (2:1, 3:2)	7-b Binary + 2:1 SC + 1:3 Dickson
Technology	180nm	250nm	32nm	180nm
Capacitor Type	MIM + MOS	MIM	Deep Trench	MIM + MOS
Capacitance (nF)	2.24	3	64	3
Input Range	3.4~4.3V	2.5V	1.8V	0.9~5V
Output Range	>0.45V	0.1~2.18V	0.7~1.1V	0.6, 1.2, 3.3V (regulated)
Number of Conversion Ratios	117	15	2	127 × 2(up/down)
Load Range	300uA	2mA	10W	20nW~500uW @ >60%
Clock Frequency	80kHz~2.7MHz	200kHz~10MHz	<62.5MHz	50Hz~10MHz (sim)
Peak Efficiency	72%	85%	85.1%	81%

Figure 8.5.6.
Performance summary and comparison.

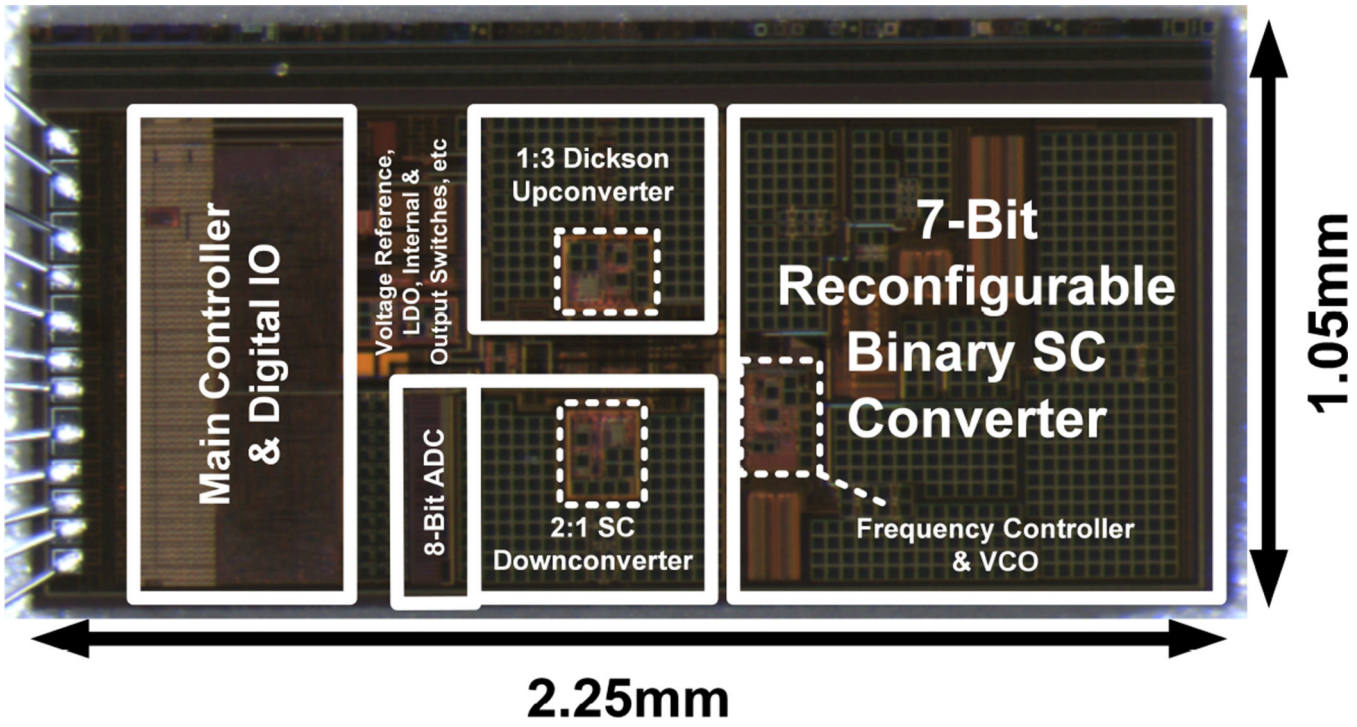

Figure 8.5.7.
Die micrograph.