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# Accurate extraction of WSe2 FETs parameters by using pulsed I-V method at various temperatures

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## Abstract

This work investigates the intrinsic characteristics of multilayer $WSe_2$ field effect transistors (FETs) by analysing Pulsed *I-V* (PIV) and DC characteristics measured at various temperatures. In DC measurement, unwanted charge trapping due to the gate bias stress results in *I-V* curves different from the intrinsic characteristic. However, PIV reduces the effect of gate bias stress so that intrinsic characteristic of $WSe_2$ FETs is obtained. The parameters such as hysteresis, field effect mobility ($\mu_{eff}$), subthreshold slope (*SS*), and threshold voltage ($V_{th}$) measured by PIV are significantly different from those obtained by DC measurement. In PIV results, the hysteresis is considerably reduced compared with DC measurement, because the charge trapping effect is significantly reduced. With increasing temperature, the field effect mobility ($\mu_{eff}$) and subthreshold swing (*SS*) are deteriorated, and threshold voltage ($V_{th}$) decreases.

**Keywords:** Two-dimensional materials, $WSe_2$ FETs, Pulsed *I-V* method, DC method, Temperature

## 1 Background

Two-dimensional(2D) layered materials such as graphene and boron nitride offer new opportunities in the field of electronics with its excellent physical, chemical properties [1–6]. Though graphene has been studied most widely, its lack of bandgap limits its application. Transition metal dichalcogenides (TMDCs) provide a solution to this problem with their sizable bandgap energy and ultra-thin form of layers. Among them, $WSe_2$ FETs can be very appealing for the nanoscale electronic applications and blackplanes for flat panel display (FPD) due to their high mobility (~100 cm²/V·s), excellent on/off ratio(~$10^7$), and low subthreshold swing (SS, ~70 mV/decade) [7–9].

When we simulate the circuits which consist of $WSe_2$ FETs, it is necessary to know the parameters of the FETs. Most of the parameters reported up to now were extracted from the *I-V* characteristics obtained by the DC method. However, these values were not correct, because a large hysteresis is observed due to the gate bias

stress during the DC measurement [10–12]. On the other hand, in the Pulsed *I-V* (PIV) measurement, the effect of gate bias stress is reduced greatly so that intrinsic characteristic of $WSe_2$ FETs can be obtained [13, 14]. Thus PIV method is considered as a reasonable method for estimating the performance and reliability of semiconductor devices. The purpose of PIV method is to avoid the negative effects such as self-heating and transient trapped charges. Therefore, the PIV method can provide the accurate device parameters needed for improved computer-aided-engineering (CAE) software models. However, there have been no reports on the parameter extraction from the fabricated $WSe_2$ FETs at various temperatures. In this work, we show the *I-V* curves measured by PIV and DC measurement methods, and compare the parameters extracted from the results obtained by both methods at various temperatures (−30 to 40 °C).

## 2 Experimental details

Figure 1 shows the perspective view of the structure of a multilayer $WSe_2$ FET with the bottom gate structure. An *n*-type silicon wafer which was heavily doped (ρ ~ 0.005 Ω·cm) by phosphorus is used as a starting substrate and also plays a role as back-gate electrodes. After thermal

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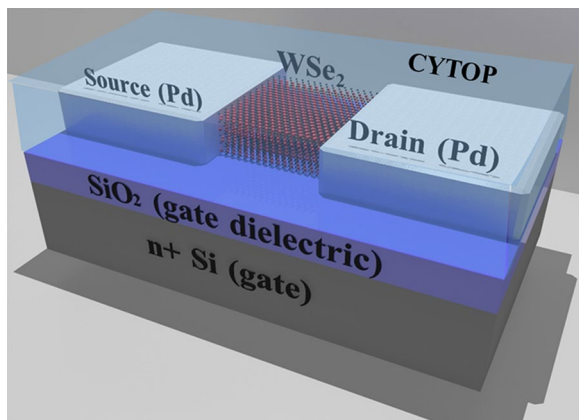
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**Fig. 1** Schematic diagram of multi-layer $WSe_2$ FETs with a heavily *n*-doped Si bottom-gate and Pd source/drain contact



**Fig. 2** Comparison of $I_D$-$V_{GS}$ characteristics of a $WSe_2$ FET measured by DC method and PIV ($t_{on} = 10^{-4}$ s, $t_{off} = 1$ s, $V_{base} = 0$ V) methods at 20 °C

oxidation in dry oxygen at 950 °C, 35 nm thick thermal oxide which serves as gate insulator was grown on the heavily doped Si wafer. Then, $WSe_2$ flakes were mechanically exfoliated from bulk $WSe_2$ crystals and transferred on $SiO_2$/Si substrate by using a polydimethylsiloxane (PDMS) stamp. The multi-layer $WSe_2$ flakes on the substrate were annealed at 350 °C for 2 h in the ambient of a mixed gas of argon and hydrogen. Photolithographic patterning and electron beam evaporation of Pd (~70 nm), followed by lift-off in acetone, create source and drain electrodes on the $WSe_2$ flakes with a good Ohmic contact. *However, one of the key limitations for TMDC devices, like other types of low-dimensional material, comes from the intrinsic nature of instability associated with easy adsorption of gaseous molecules such as oxygen and moisture due to the large surface areas of low-dimensional materials. Absorbed gaseous molecules and moisture can act as a charge trap site* [15]. *To prevent the molecules being absorbed, we adopted flourinated polymer (CYTOP; CTL-809 M, Asahi Glass Co., Ltd) passivation so that the drift of the drain current in $MoS_2$ FETs was reduced greatly* [16]. Therefore, the backside of the $WSe_2$ flake was encapsulated by the CYTOP with typical spin coating process. Then, after thermal evaporation of SiOx(~50 nm) on the CYTOP, for a surface promoter layer during PR coating, pad opening was completed by dry etching(~$SF_6$/$CF_4$) via PR patterns.

## 3 Result and discussion

Figure 2 shows the transfer curves ($I_D$–$V_{GS}$) measured at 20 °C from the FET with a *W/L* of 30/10 µm at a drain-to-source voltage ($V_{DS}$) of −0.1 V. We carried out the measurement using WGFMU (Waveform Generator and Fast Measurement Unit) module installed in an Agilent B1500 semiconductor parameter analyser. *In DC and PIV*
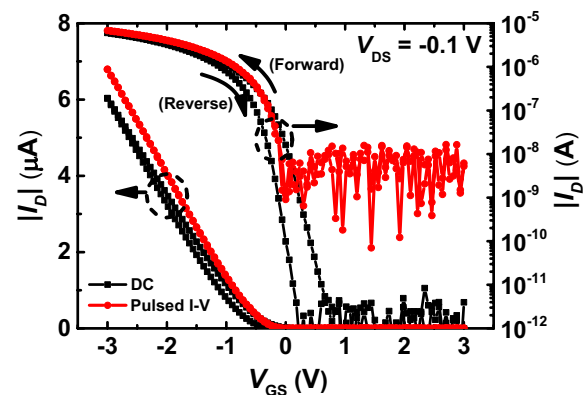
*measurement, the $V_{GS}$ is scanned from 3 to −3 V (forward) and then from −3 to 3 V (reverse).* The transfer curves obtained by DC measurement show a large hysteresis. Because of the $V_{GS}$ stress during the DC measurement, the charges can be trapped or de-trapped at the $WSe_2$/$SiO_2$ interface and/or the backside of $WSe_2$ flakes, therefore the threshold voltage ($V_{th}$) can be shifted positively or negatively. In Fig. 2, we can clearly observe the hysteresis in DC $I_D$−$V_{GS}$ curves represented by square symbols, but not in the PIV curves. The drain currents measured by the DC method are smaller than those measured by the PIV method when the $V_{GS}$ is larger than $V_{th}$ in magnitude. If we extract the carrier mobility from the DC $I_D$−$V_{GS}$ curves, the mobility seems to be degraded. Since some of the trapped charges stay trapped until the gate polarity is switched in the DC measurement, the large hysteresis is observed in DC measurement [17]. Note the off–current obtained by the PIV method is much higher than that obtained by the DC method in Fig. 2 because the low limit of the WGFMU module in measurement current is ~$10^{-8}$ A. In PIV measurement, we investigated the optimized condition to reduce gate bias stress as small as possible. Figure 3a, b depict bias scheme for the DC and Pulsed *I-V* measurements, respectively. The $t_{sw}$ in the inset of Fig. 3a represents the step width at each bias step. The drain bias ($V_{DS}$) is fixed at −0.1 V from the start of the measurement. The $t_{on}$, $t_{off}$, and $V_{base}$ in the inset of Fig. 3b stand for turn-on pulse width ($10^{-4}$ s), turn-off pulse width (1 s), and the bias during turn-off (0 V), respectively [17]. *During the period, both rise and fall times are $10^{-7}$s.* The $V_{GS}$ pulse during $t_{off}$ is set to 0 V to minimize the $V_{GS}$ stress effect. Shorter $t_{on}$ and longer $t_{off}$ are necessary to suppress the effect of the trapping and detrapping of the charges. Note the drain bias is synchronized with the gate bias and the bias is −0.1 V during $t_{on}$.
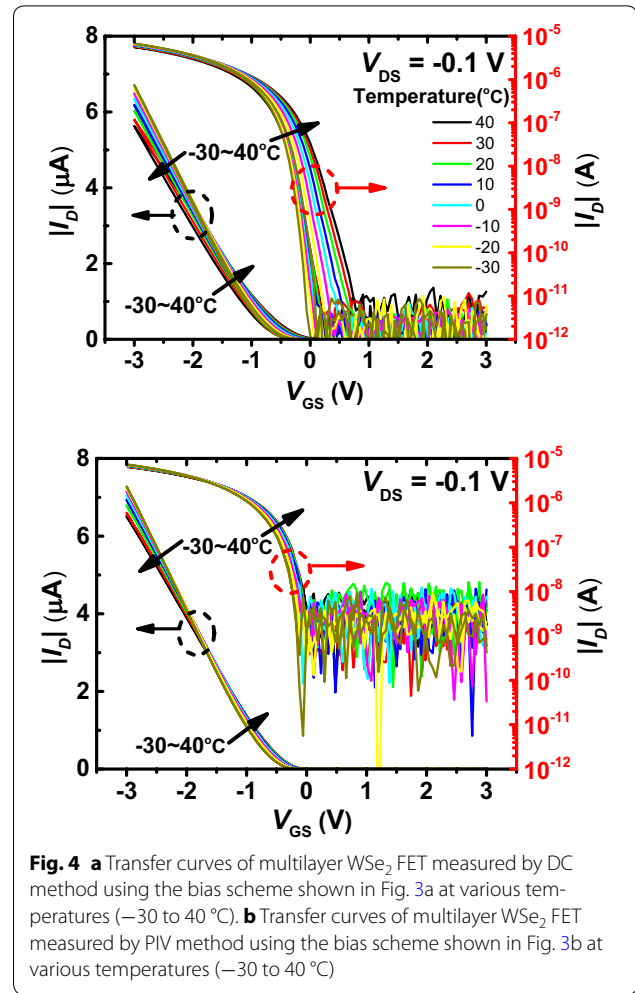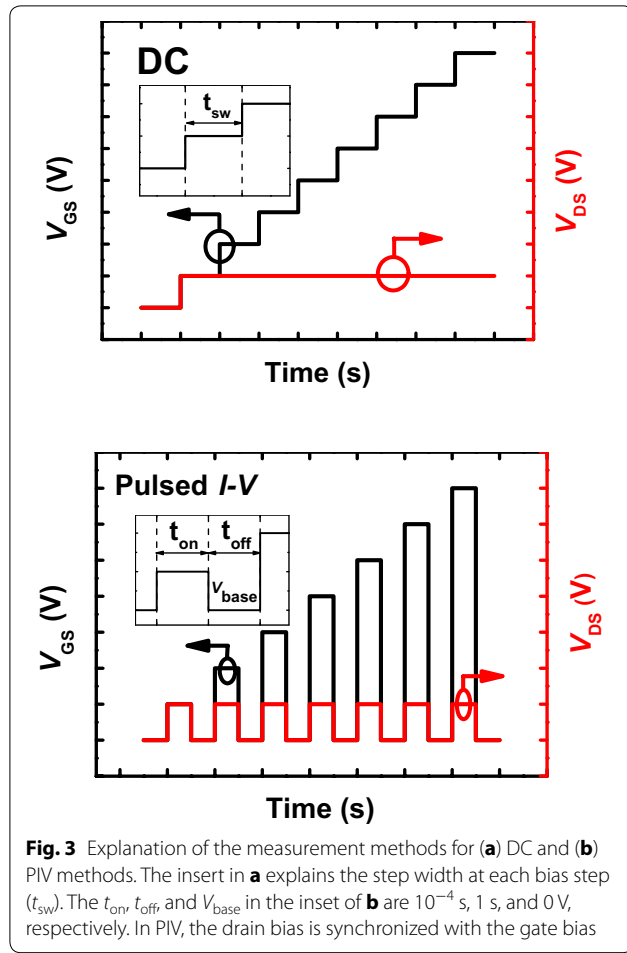
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**Fig. 3** Explanation of the measurement methods for (**a**) DC and (**b**) PIV methods. The insert in **a** explains the step width at each bias step ($t_{sw}$). The $t_{on}$, $t_{off}$, and $V_{base}$ in the inset of **b** are $10^{-4}$ s, 1 s, and 0 V, respectively. In PIV, the drain bias is synchronized with the gate bias



**Fig. 4** **a** Transfer curves of multilayer WSe$_2$ FET measured by DC method using the bias scheme shown in Fig. 3a at various temperatures (−30 to 40 °C). **b** Transfer curves of multilayer WSe$_2$ FET measured by PIV method using the bias scheme shown in Fig. 3b at various temperatures (−30 to 40 °C)

Figure 4a, b show the transfer curves measured by DC and PIV methods, respectively, at various temperatures at a $V_{DS}$ of −0.1 V. As mentioned in Fig. 2, the hysteresis is much suppressed by measuring the device with the PIV method. Mobility ($\mu_{eff}$), subthreshold swing (*SS*), $V_{th}$ are extracted from the transfer curves at various temperatures.

In Fig. 5, shown is temperature dependency of electrical parameters extracted from transfer curves of multilayer WSe$_2$ FETs. In Fig. 5a, the hysteresis is clearly observed in the $I_D-V_{GS}$ curves obtained by DC method, but ignorable hysteresis in the curves measured by PIV method. The hysteresis was defined as the $V_{GS}$ difference at a fixed drain current of $10^{-8}$ A between the forward and reverse scans. Electrons or holes during the measurement of the DC method can be trapped or detrapped into the traps at the interface due to $V_{GS}$ stress, which leads to a positive or negative shift in the $V_{th}$. As the temperature increases, the hysteresis in the curves measured by DC method increases because elevated temperature activates the trapping and detrapping process of carriers.

It seems that the time constants for the carrier trapping and detrapping in given temperature range are longer than the $t_{on}$ ($10^{-4}$ s) used in this work so that the increase of hysteresis during PIV method can be ignorable. The variation of the hysteresis with the $t_{on}$ was studied in [17].

Figure 5b shows the temperature dependency of mobility. The field effect mobility was extracted from the maximum point of transconductance ($g_m$) using the following equation

$$\mu_{eff} = \frac{Lg_m}{WC_iV_{DS}} \tag{1}$$

where C and $g_m$ are gate capacitance per unit area and the transconductance, respectively. The $\mu_{eff}$ was deteriorated as the temperature increases from −30 to 40 °C. Phonon scattering is enhanced with rising temperature, which leads to the degradation in the carrier mobility. According to the relation of $\mu_{eff} \propto T^{-\gamma}$, the $\gamma$s for the forward and reverse scans are 1.149 and 0.682, respectively. However, the decrease rate obtained by the PIV is

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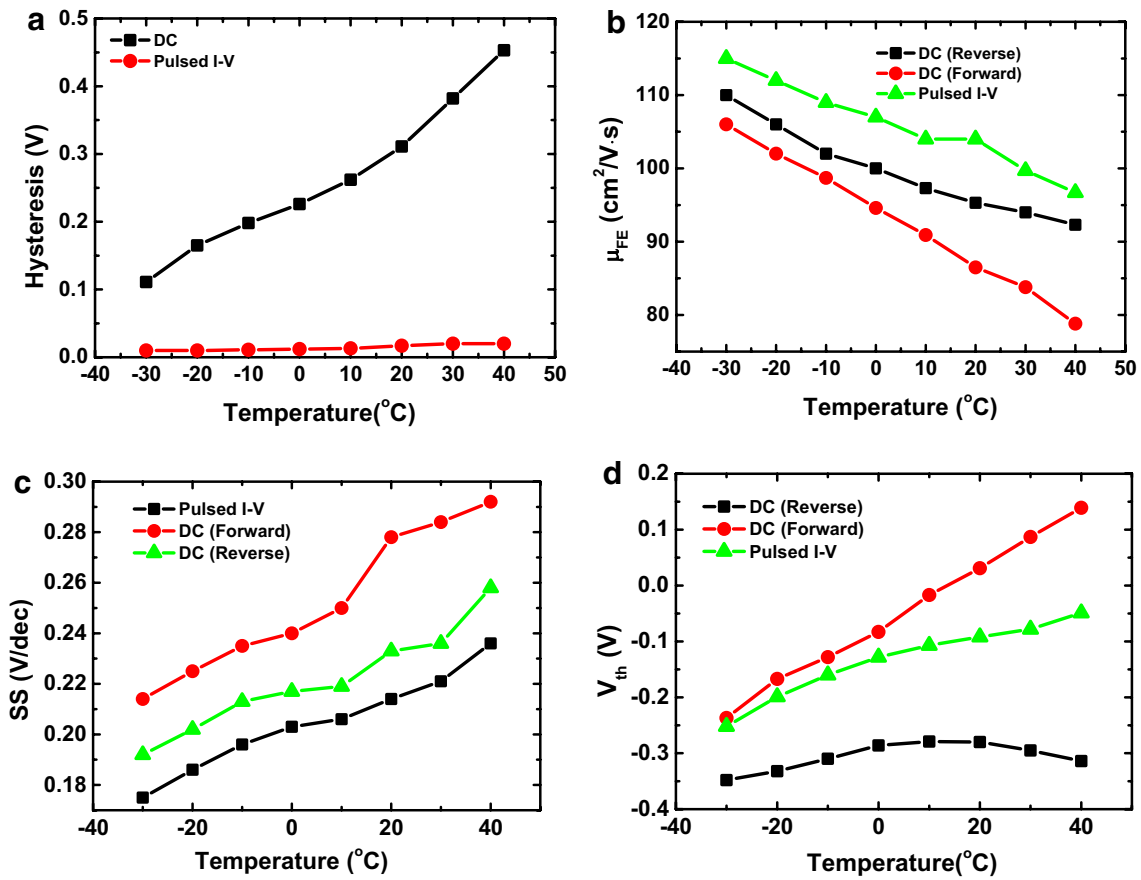
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**Fig. 5** Temperature dependency of **a** hysteresis, **b** field effect mobility, **c** subthreshold swing, **d** threshold voltage obtained from multilayer WSe$_2$ FET. All parameters are extracted from transfer curves

0.646. The mobility measured by PIV method is greater than the mobility measured by DC method, because in the DC measurement hole was trapped and it decreases the current, which decreases apparently the effective mobility. However, in Pulsed *I-V* measurement, the trapped hole was detrapped during $t_{off}$ and the mobility was not degraded appreciably. Besides, mobility measured in DC forward scan is lower than the mobility measured in DC reverse scan. The hole density in the channel is reduced due to the charge (hole) trapping during DC forward scan, so the slope of *I-V* curves is reduced, which results in reduced mobility. During DC reverse scan, the discharging is mainly occurred by hole emission to the valance band. The holes need some energy to be emitted to the valence band. Therefore, the traps do not discharge significantly until the gate bias is below threshold voltage ($V_{th}$), so the carrier density in the channel is reduced.

In addition, as the temperature rises, the difference between the mobility measured by DC forward and reverse scans increases as shown in Fig. 5b. The reason

for the difference is explained as follows. Compared to the case of the forward scan, the holes in the reverse scan are increasingly emitted to the valence band with increasing temperature since increasing temperature increases the energy of the holes trapped.

Figure 5c shows subthreshold swing (*SS*) measured at various temperatures. The *SS* was defined as $V_{GS1}$($V_{GS}$ at $I_d = 10^{-9}$ A)−$V_{GS2}$($V_{GS}$ at $I_d = 10^{-8}$ A). As temperature increases, the *SS* increases as given by

$$SS = 2.3\frac{kT}{q}\left(1 + \frac{C_{dm}}{C_{ox}}\right). \qquad (2)$$

*SS* measured by DC measurement is greater than *SS* measured by PIV, because charge trapping decreases the current in DC measurement which makes *SS* larger. Furthermore, *SS* measured by DC forward scan is larger than the *SS* measured by DC reverse scan, because as explained above the slope of DC forward scan is smaller than that of DC reverse scan. The difference between *SS* measured by DC forward scan and *SS* measured by DC reverse scan increases as temperature rises. This

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phenomenon can be explained by the physics explained in the mobility difference with the temperature.

The threshold voltage ($V_{th}$) was calculated by reading a gate-source voltage ($V_{GS}$) at a constant current ($I_d = 10^{-8}$ A). In PIV method, the threshold voltage shifts to the positive direction due to the increase of thermally activated carrier density. At any temperature, the threshold voltage measured by DC forward scan is in the rightmost position, and the threshold voltage measured by DC reverse scan is in the leftmost position. The reason can be explained as follows. During DC forward scan, the electron was trapped before $V_{GS}$ reaches $V_{th}$ so the threshold voltage moves to the right. On the other hand, during DC reverse scan, the hole was trapped before $V_{GS}$ reaches $V_{th}$ so the threshold voltage moves to the left. Furthermore, the difference between $V_{th}$s measured by DC forward and reverse scans increases with increasing temperature, since the hysteresis increases.

## 4 Conclusions

In this paper, we extracted key parameters of WSe$_2$ FETs accurately at various temperatures by adopting pulsed *I-V* (PIV) method. The behavior of these parameters are different from that of the parameters obtained by DC method. For example, the decrease rates of the hole mobility are 1.149 and 0.646, respectively, for DC (forward scan) and PIV methods. By using PIV method, we could obtain accurate behavior of hysteresis, hole mobility, subthreshold swing, and threshold voltage with increasing temperature. We observed notable degradation of parameter with increasing temperature. The mobility is degraded, subthreshold swing increases and threshold voltage moves to the right as temperature rises. The parameters obtained by using PIV method are accurate and will be useful in the simulation of WSe$_2$ FETs circuit at various temperatures.

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