Published in final edited form as:

Dig Tech Pap IEEE Int Solid State Circuits Conf. 2016 ; 2016: 218–219. doi:10.1109/ISSCC.2016.7417985

A Rational-Conversion-Ratio Switched-Capacitor DC-DC Converter Using Negative-Output Feedback

Wanyeong Jung, **Dennis Sylvester**, and **David Blaauw**

University of Michigan, Ann Arbor, MI

Switched-capacitor (SC) DC-DC converters have several advantages over inductive DC-DC converters in that they are easily integrated on-chip and can scale to desired power levels, rendering themselves promising for integrated voltage regulators, especially for small, low-power systems. However, many SC DC-DC converters offer only a few conversion ratios, limiting their use for systems in which either the input and output voltages vary. This is particularly important in wireless systems where battery voltage degrades slowly. [1] proposed a technique to reconfigure cascaded SC converters to achieve arbitrary binary ratios: $p/2^N$, $0<p<2^N$, where N is the number of cascaded stages. This structure was improved in [2] by reversing the cascading order to increase output conductance and in [3] by using a positive feedback approach. However, this design still provides less output conductance than previous works offering only a small fixed number of ratios [4,5]. This paper presents an SC DC-DC converter that can be reconfigured to have any arbitrary rational conversion ratio: p/q, $0<p<q\leq 2^{N+1}$. The key idea of the design, which we refer to as a rational DC-DC converter, is to incorporate negative voltage feedback into the cascaded converter stages using negative-generating converter stages ("voltage negators"); this enables reconfiguring of both the numerator p and denominator q of the conversion ratio. With help from the current supply of the voltage negators, output conductance becomes comparable to conventional few-ratio SC DC-DC designs. Hence, the proposed design achieves a resolution higher than previous binary SC converters while maintaining the conversion efficiency of dedicated few-ratio SC converters. Using only 3 cascaded converter stages and 2 voltage negator stages, the rational converter implemented in 180nm CMOS offers 79 conversion ratios and achieves >90% efficiency when downconverting from 2V to a 1.1−1.86V output voltage range.

Fig. 12.1.1 shows the structure of the rational converter, with comparison to a conventional binary-reconfigurable DC-DC converter [2]. In the binary converter, each stage has a 2:1 SC converter that receives one input from the previous stage's output, and the other from a power supply rail, either VDD or VSS. Since each 2:1 converter has 1/2 voltage gain from input to output, changing supply voltage at a stage far away from the output has an exponentially smaller impact than ones near the output, resulting in binary ratio tuning.

In a rational converter (Fig. 12.1.1), one input of each 2:1 SC downconverter is connected to the output of the previous stage, as in the binary converter. However, the other input is chosen among the supply rails as well as a set of negative feedback voltages, $-V_{OUT}$, $VDD-V_{OUT}$, and $2VDD-V_{OUT}$ so that V_{OUT} is determined by an equation $V_{OUT}=A\times VDD - B\times V_{OUT}$, where A and B are referred to as the converter's forward path gain and feedback

factor, respectively. Negative voltage feedback enables three extra choices for each stage, increasing the number of combinations and thus its reconfigurability – this allows the converter to be reconfigured in an algorithmic way to any rational conversion ratio p/q, $0<p<q\leq 2^{N+1}$, where N is the maximum number of 2:1 stages. In addition, the negating converters provide extra current into the output terminal, improving overall converter output conductance. For any rational conversion ratio, the normalized conductance of the rational converter is provably no smaller than previous (incl. few-ratio) SC converters. In addition, switching loss in the rational converter matches previous best reported SC converters at many ratios and hence leads to similar or better overall efficiency.

Fig. 12.1.2 describes operation of the rational converter in more detail using two examples. First, when the conversion ratio is set to p/q = 4/13 (Fig. 12.1.2, top), the number of stages N is set by p and q to be three as 4/13 can be represented as a ratio of two binary fractions with three digits after the binary point, $0.100_{(2)}$ / $1.101_{(2)}$. The numerator of this ratio becomes the forward path gain *A*, and the denominator minus one, $0.101_{(2)}$, becomes the feedback factor *B*. The input supply voltage of each stage is selected by the corresponding digits in the binary representation of *A* and *B,* i.e., a_i and b_i. Specifically the *i*th converter stage uses the *i*th bit from the right in *A* or *B* and selects an input voltage equal to $a_i \times VDD - b_i \times V_{OUT}$, which effectively gives the four options of VDD, VSS, VDD−V_{OUT}, and −V_{OUT}. In this manner the converter can be configured for any *A* and *B*, provided *A* is less than 1.

For $A \geq 1$, the voltage negators are reconfigured to generate VDD−V_{OUT} and 2VDD−V_{OUT}. For example, when the conversion ratio p/q is 9/11 as shown in Figure 12.1.2 (bottom), N is set to three as 9/11 = $1.001_{(2)}$ / $1.011_{(2)}$, and *A* is $1.001_{(2)}$ and *B* is $0.011_{(2)}$ accordingly. With the change in voltage negator configuration, the voltage selection signal for forward path gain is also changed into a new value *A*' × *A*-*B*, which is always less than 1 if p<q. To compensate for the reduction in forward path gain by *B*, extra VDD is added whenever b_i is 1 by selecting $a'_i \times VDD - b_i \times (V_{OUT} - VDD)$ among VDD, VSS, VDD−V_{OUT}, and 2VDD −V_{OUT}. In the example case of p/q = 9/11, *A*' becomes $A-B = 0.110_{(2)}$, which is actually realized in the converter by setting a'_L=1, a'_1=1, a'_2=0 and a'_3=1 because this configuration offers lower bottom-plate parasitic switching loss than setting a'_L=0, and a'_1, a'_2, and a'_3 to 0, 1, 1, respectively.

Fig. 12.1.3 shows a theoretical analysis of the rational converter with a comparison to the recursive binary converter [2]. The rational converter offers many more conversion ratios due to both numerator and denominator being selectable, and this number increases faster than binary converters as more stages are cascaded. Many of these non-binary ratio configurations have higher conductance than binary configurations for similar voltages, and thus, lower conduction loss. For every configuration, the rational converter has an output conductance of $I_{OUT}/\Delta V = C_{FLY}F_{CLK} \times q^2/(q-1)^2$ when assuming the output is a DC voltage, which marks the best conductance among SC converters that do not include inductors. Furthermore, the flexibility in selecting a_L and b_L in the first stage can be exploited to reduce bottom plate swing in many conversion ratios, further lowering bottom plate switching loss. Therefore, a rational converter guarantees higher or equal efficiency relative to a binary converter over the entire output voltage range. This statement holds even

assuming infinite stages in the binary converter since most added ratios in this case offer poor efficiency arising from increased conduction loss.

To test the performance of this converter and fairly compare it with other previous converters, a generally reconfigurable SC converter is designed as shown in Fig. 12.1.4. It consists of 15 identical unit converters that can form into an up to 4-stage binary converter with 15 ratio configurations ($p/2^4$, $0<p<2^4$), a few-ratio converter with 1/3 and 2/5 ratios, or an up to 3-stage rational converter with 79 ratio configurations (p/q, $0<p<q\leq 2^4$), with relative sizing among stages for optimal normalized conductance. The unit converter is a 2-phase SC converter with four terminals that can be a 2:1 converter or a voltage negator. Each terminal can be connected to arbitrary voltage rails including VDD, VSS, V_{OUT}, negative feedback voltages, and three intermediate voltages for inter-stage connections. Despite the large number of reconfiguration switches, they do not impact efficiency as they all form connections among DC voltages and hence do not contribute additional switching loss.

A test chip including the general reconfigurable DC-DC converter described above was fabricated in 180nm CMOS (die photo in Fig. 12.1.7). An input voltage of 2V is used and the converter includes a total capacitance of 1.8nF (0.12nF ×15). As shown in Fig. 12.1.5 (top left), the rational DC-DC converter has more ratios and higher conversion efficiency than previous binary converters, which is consistent with theoretical calculations in Fig. 12.1.3. The top right graph in Fig. 12.1.5 compares the output conductance at 2/3 configuration of the rational converter with the most similar ratio configuration of the binary converters, 11/16, showing that 2/3 configuration has higher output conductance, and thus, better efficiency. When compared to some previous few-ratio converters' configurations [4, 5] (Fig. 12.1.5, bottom), the rational converter has similar or better conductance and efficiency. The converter has 95% peak conversion efficiency for V_{OUT} of 1.83V, >90% efficiency over a range of V_{OUT} from 1.1V to 1.86V, and >80% efficiency over a wide 0.47–1.87V V_{OUT} range. Fig. 12.1.6 summarizes rational converter performance and compares it to previous related work.

References

1. Bang S, et al. A Fully Integrated Successive-Approximation Switched-Capacitor DC-DC Converter with 31mV Output Voltage Resolution. ISSCC. 2013
2. Salem LG, et al. An 85%-Efficiency Fully Integrated 15-Ratio Recursive Switched-Capacitor DC-DC Converter with 0.1-to-2.2V Output Voltage Range. ISSCC. 2014
3. Salem LG, et al. A Battery-Connected 24-Ratio Switched Capacitor PMIC Achieving 95.5%-Efficiency. VLSI. 2015
4. Le H-P, et al. A Sub-ns Response Fully-Integrated Battery-Connected Switched-Capacitor Voltage Regulator Delivering 0.19W/mm2 at 73% Efficiency. ISSCC. 2013
5. Jiang J, et al. A 2-/3-Phase Fully Integrated Switched-Capacitor DC-DC Converter in Bulk CMOS for Energy-Efficient Digital Circuits with 14% Efficiency Improvement. ISSCC. 2015

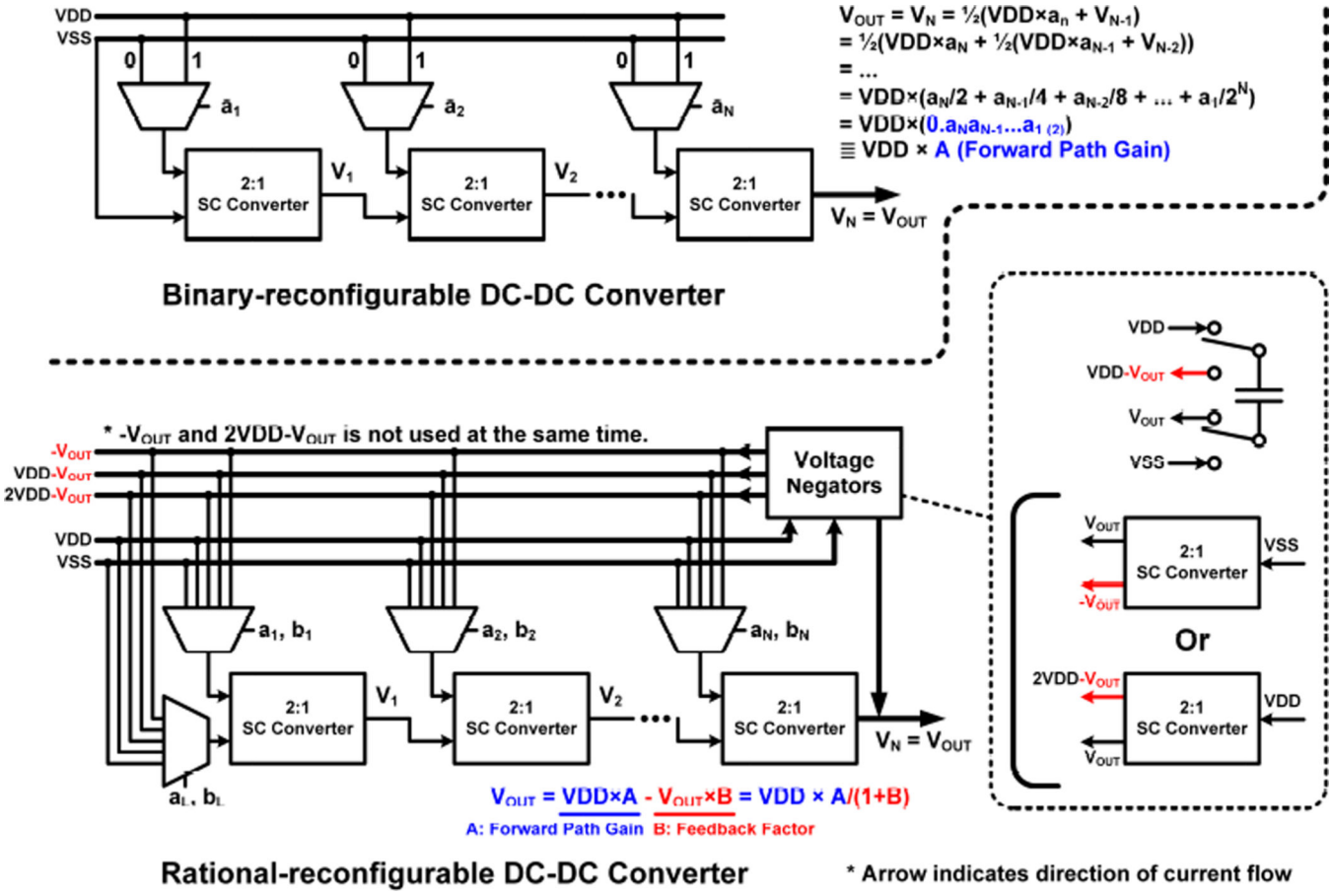


Figure 12.1.1.
Structure of the rational-conversion-ratio-reconfigurable (rational) DC-DC converter.

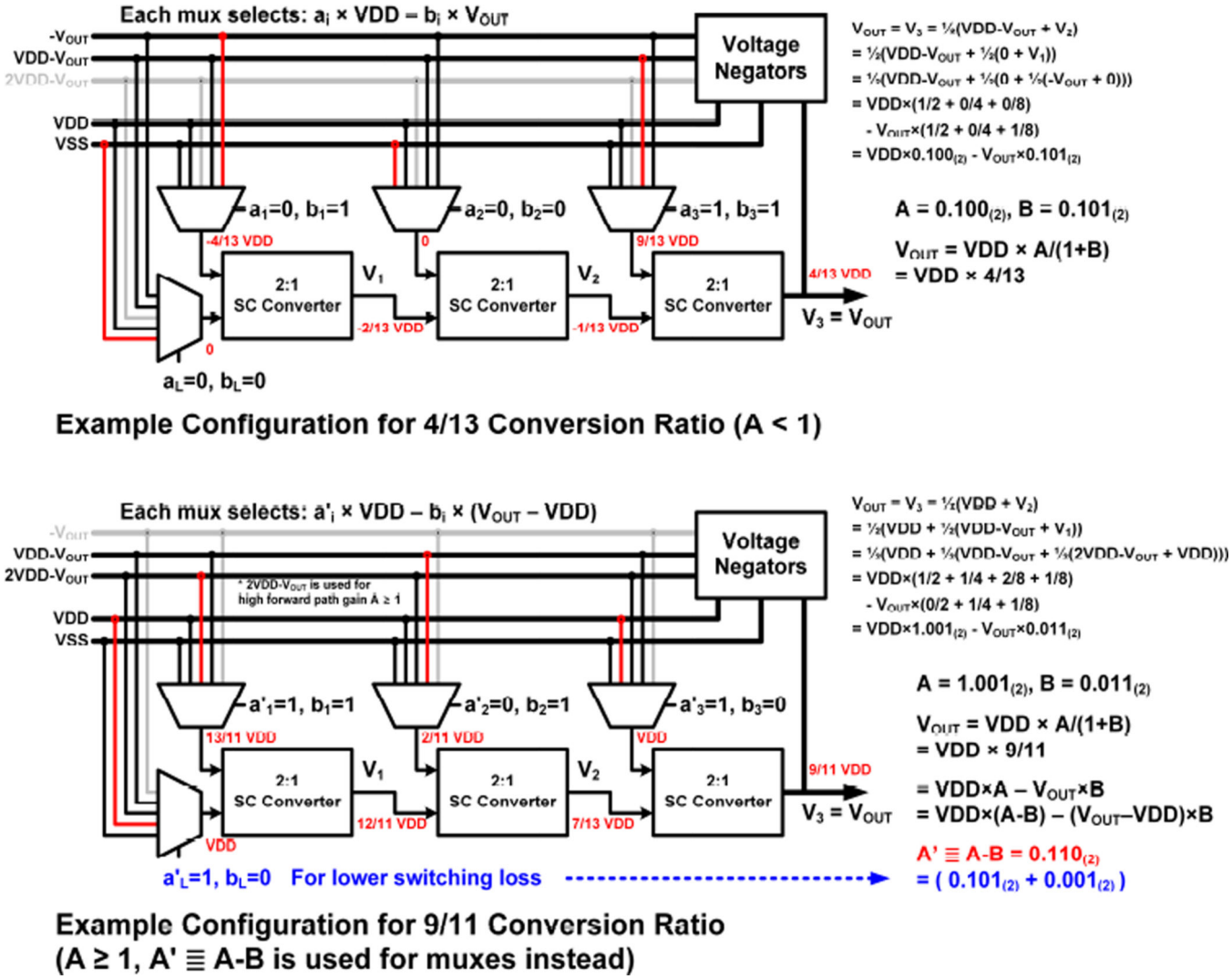
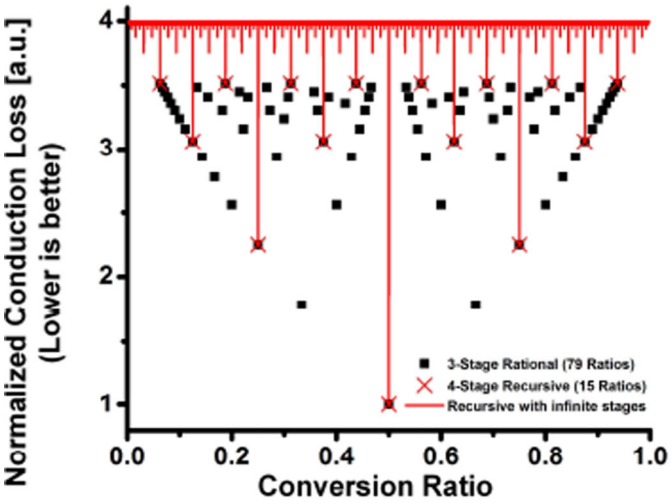
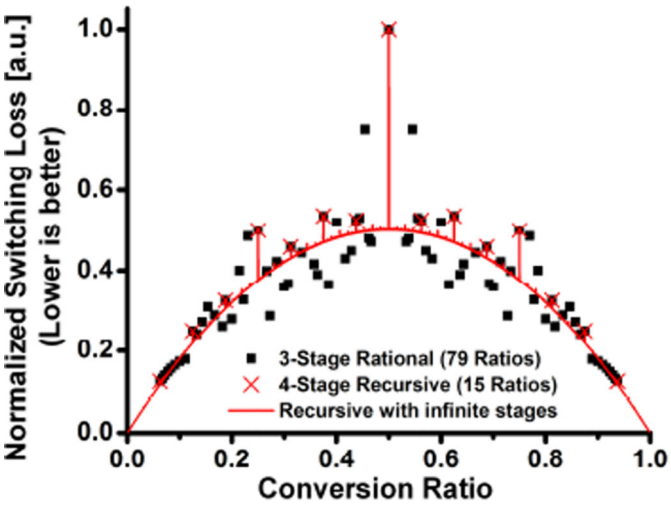


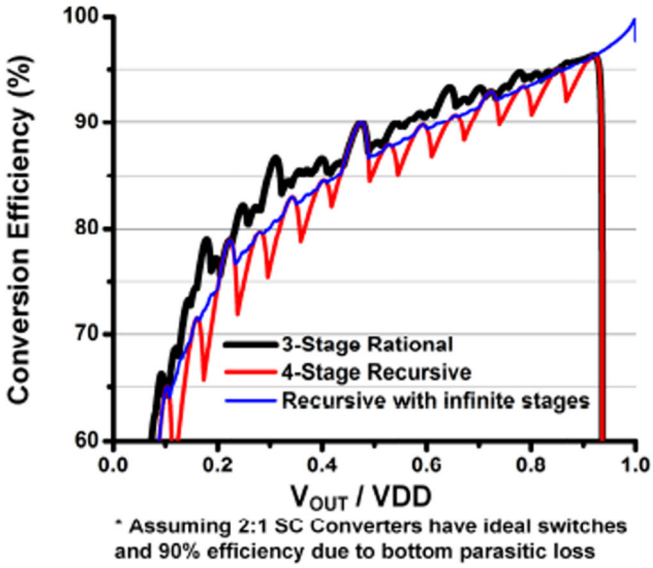
Figure 12.1.2.
Configuration examples of the rational converter for 4/13 (top) and 9/11 (bottom) conversion ratio.



Max. Stages[1]	This work (Rational)		Conventional Binary (Recursive)	
	Ratios	Stage size granularity[2]	Ratios	Stage size granularity[2]
1	5	1/3	1	1/1
2	21	1/7	3	1/3
3	79	1/15	7	1/7
4	323	1/31	15	1/15
5	1259	1/63	31	1/31
6	5021	1/127	63	1/63
7	19947	1/255	127	1/127

1. Number of main stages w/o negators for rational
2. Required stage size granularity for optimum conductance





* Assuming 2:1 SC Converters have ideal switches and 90% efficiency due to bottom parasitic loss

Figure 12.1.3.
Theoretical calculation of number of ratios, conduction loss, switching loss, and efficiency with comparison to a conventional binary DC-DC converter.

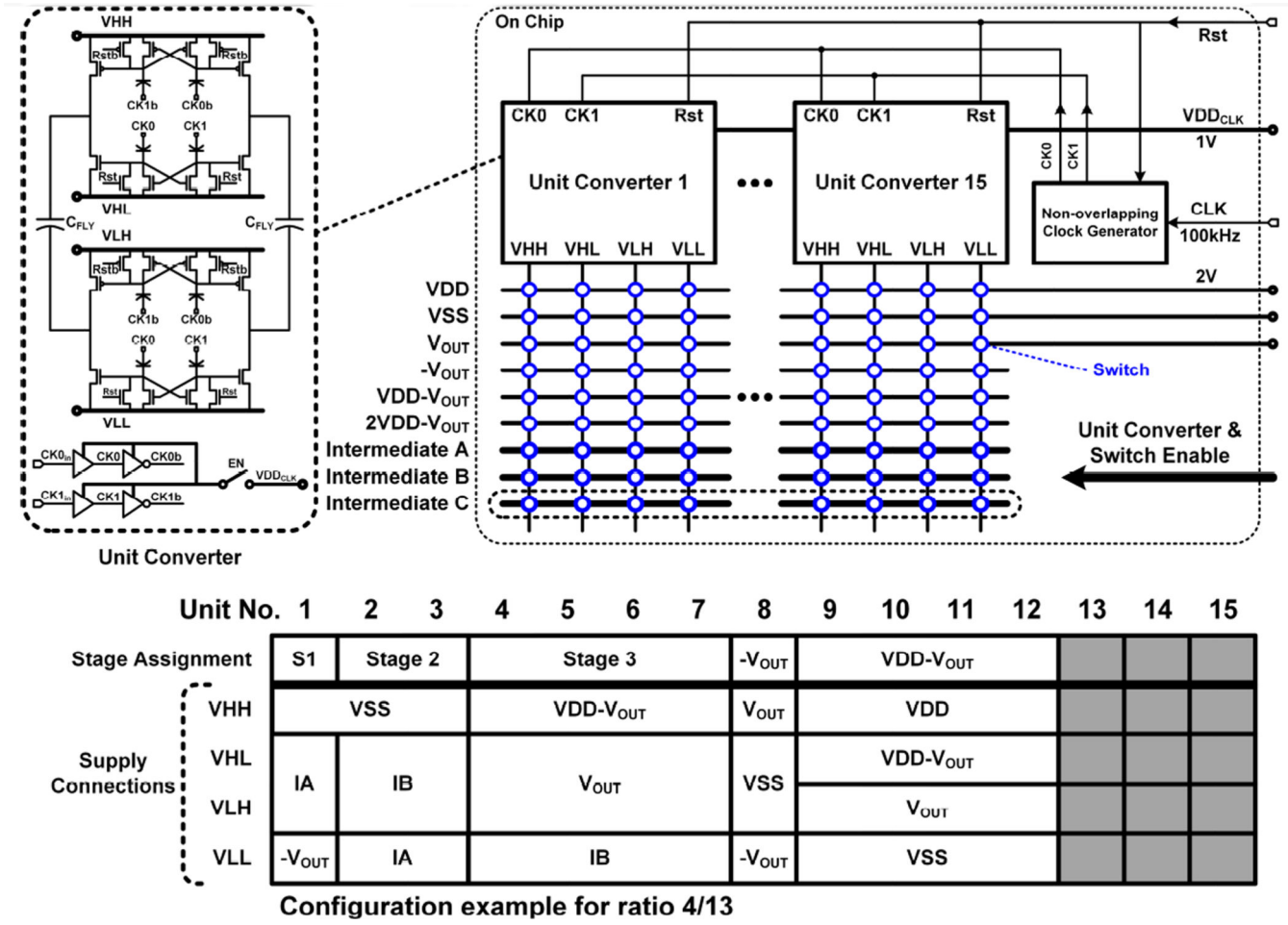


Figure 12.1.4.
Structure of general reconfigurable DC-DC converter and its configuration scheme.

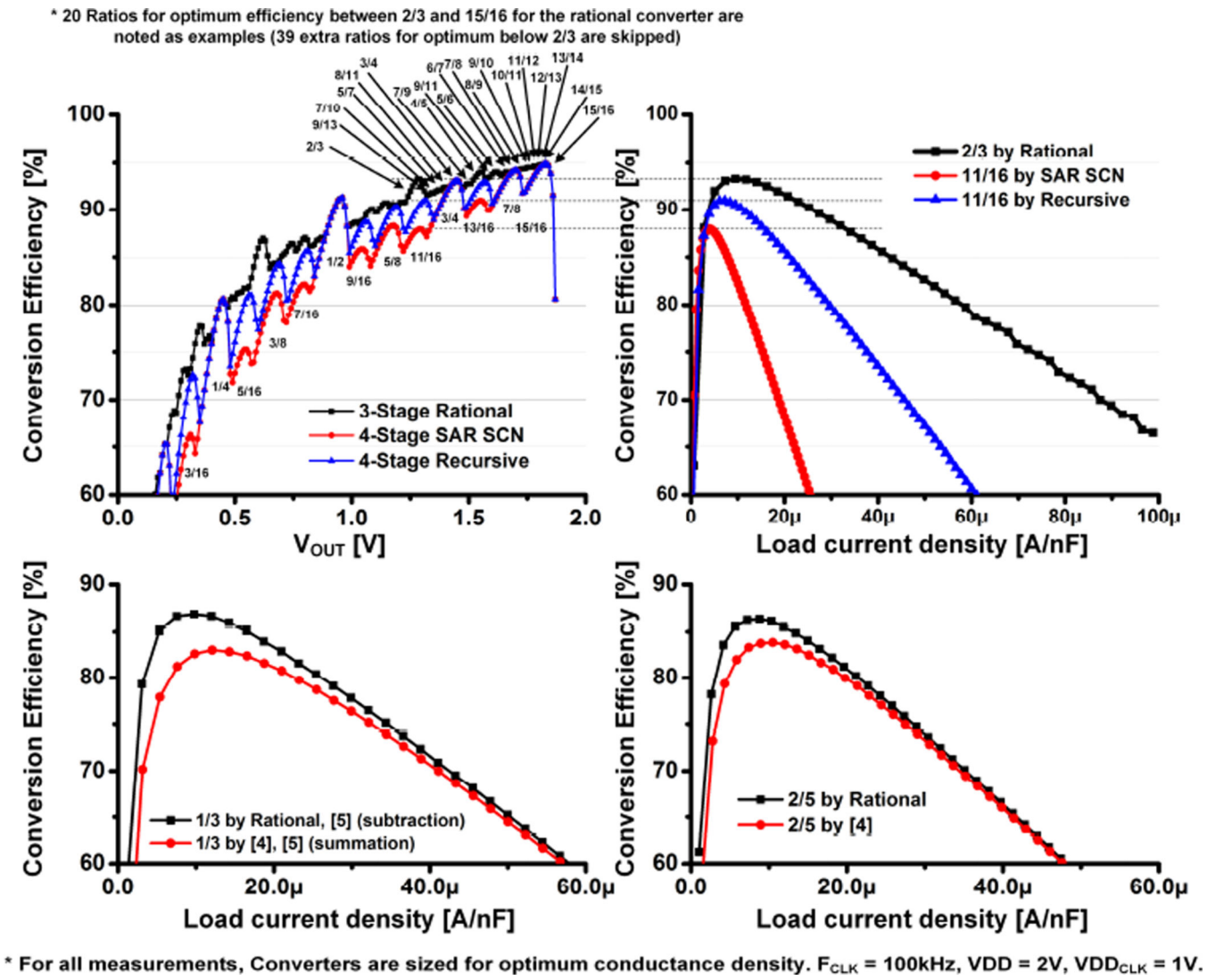


Figure 12.1.5.
Measured results of rational converter with comparison to configurations used in prior work.

	This Work	SAR SCN [1]	Recursive [2]	Salem VLSI`15 [3]	Le ISSCC`13 [4]	Jiang ISSCC`15 [5]
Technology	0.18μm CMOS	0.18μm CMOS	0.25μm CMOS	0.25μm CMOS	65nm CMOS	65nm CMOS
Fully Integrated	Yes	Yes	Yes	No	Yes	Yes
Reconfigurability Type	Rational	Binary	Binary	Gear Train + Charge Feedback	Fixed (1/3, 2/5)	Fixed (1/3, 1/4)
All-Ratio Reconfigurability	Yes	No	No	No	No	No
Number of stages	3 + voltage negators	5 + 4:1 SC	4	4 + 1	N/A	N/A
Number of Configurations	79	117	15	24	2	2
Input Voltage	2V	3.4V-4.3V	2.5V	2.5V–5V	3V-4V	1.5-2.5V
Output Voltage	1.1V-1.86V @ >90% η 0.47–1.87V @ >80% η	0.9V-1.5V	0.1V-2.18V	0.2V-2V	1V	0.4-0.7V
Peak Efficiency	95%	72%	85%	95.5%	74.3%	79.5%
Power Density @ η_{PEAK}	71.4μA/mm² @ 2MHz [1]	6μA/mm² [2]	0.43mA/mm²	2.88mA/mm² [2,3]	0.19mA/mm²	56mA/mm²

1. Measured results has low power density because the chips are mainly designed for fair comparison between various configurations under the same well-controlled conditions.

2. Estimated number from the paper.

3. With off-chip capacitors.

Figure 12.1.6.
Performance summary and comparison.

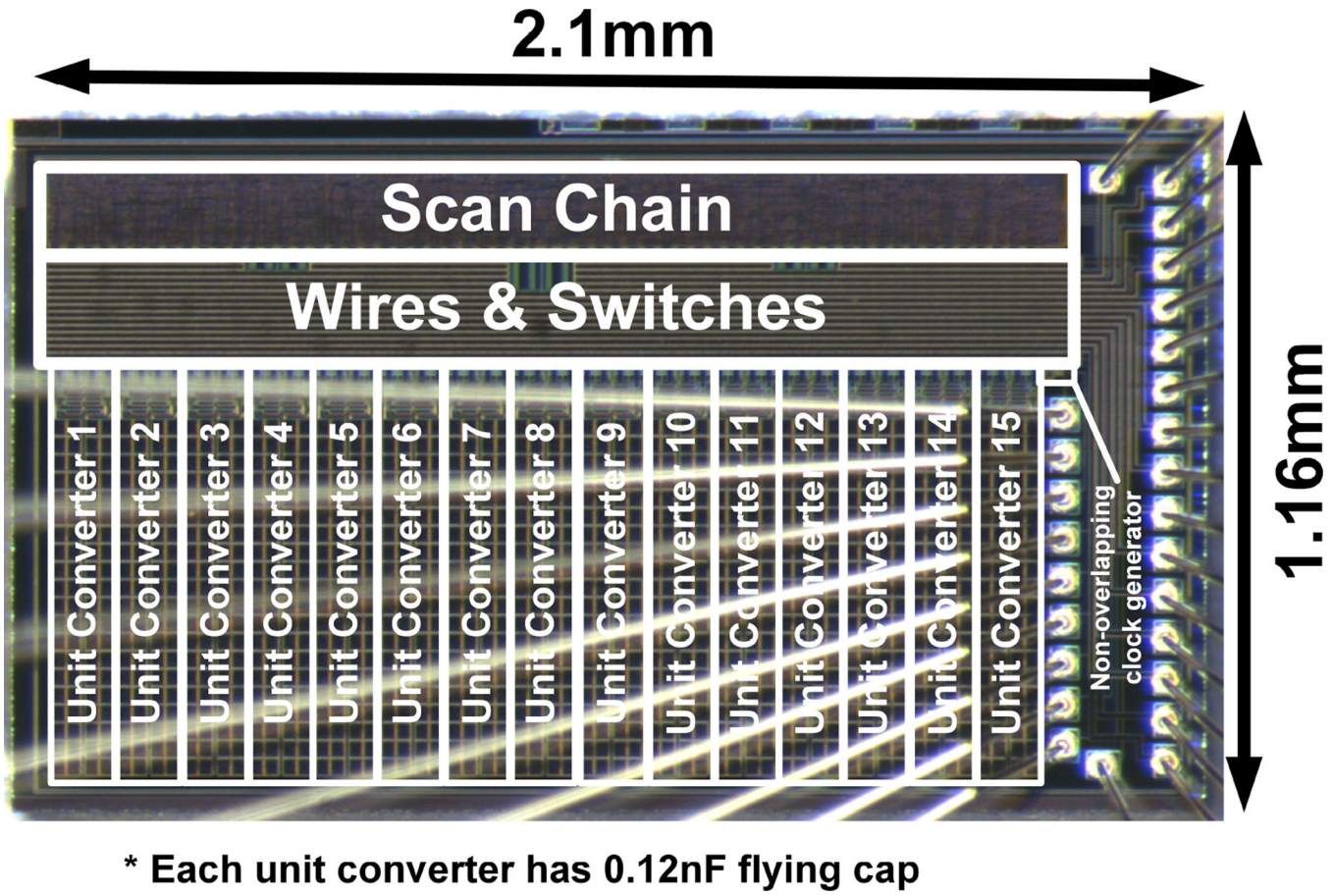


Figure 12.1.7.
Test chip micrograph.