

## Research Article

# Design, Simulation, and Experimental Verification of a Destruction Mechanism of Transient Electronic Devices

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To quickly destroy electronic devices and ensure information security, a destruction mechanism of transient electronic devices was designed in this paper. By placing the Ni-Cr film resistance and the energetic material between the chip and the package and heating the resistance by an electric current, the energetic material expanded and the chip cracked. The information on the chip was destroyed. The author simulated the temperature distribution and stress of the power-on structure in different sizes by ANSYS software. The simulation results indicate that the chip cracks within 50 ms under the trigger current of 0.5 A when a circular groove with an area of 1 mm<sup>2</sup> and depth of 0.1 mm is filled with an expansion material with an expansion coefficient of 10<sup>-5</sup>°C<sup>-1</sup>. Then, the author prepared a sample for experimental verification. Experimental results show that the sample chip quickly cracks and fails within 10 ms under the trigger current of 1 A. The simulation and experimental results confirm the feasibility of the structure in quick destruction, which lays the foundation for developing instantaneous-failure integrated circuit products to meet information security applications.

## 1. Introduction

With the rapid development of semiconductor technology, electronic technology has brought unparalleled convenience to people's life by accelerating and improving the acquisition, storage, and transmission of information. As physical carriers of information and technology, electronic components are related to the security of core information and key technologies of military equipment and are the hard power to guarantee the security of the "fifth territory"—cyberspace, after land, sea, air, and sky [1]. Traditionally, the core electronic components are destroyed by high-pressure burning, quick wiping [2], or encryption algorithm [3] method to ensure information security. However, for the high-pressure burning method, there is a hidden danger of incomplete damage to core components; for the quick erasing method, the information may be recovered because of incomplete erasing; for the encryption algorithm method, as the algorithm and other core technical information are

stored in the physical carrier of equipment, security problems may occur at the device level [4].

Professor John A. Rogers [5] of the University of Illinois at Urbana-Champaign published an article in *Science* in 2012, proposing the concept of transient electronics, which has brought a new "dawn" to the chip security technology needed by information security. However, there are some unavoidable and difficult technical obstacles for the transient electronic technology based on degradation and disappearance in practical application, including the following aspects: first, the introduction of biodegradable materials makes the packaging and structure of devices different from that of conventional electronic devices fundamentally, which is difficult to meet the requirements of conventional electronic devices, especially for military electronic devices that are resistant to high temperature, cold, acid, and alkali, and even radiation and other harsh application environments; second, a transient electronic device should be equipped with ultrathin core part and even must adopt such device

types as thin-film electronic and organic electronic, which restricts the applicable scene of transient electronic devices seriously and makes them difficult to meet the application requirements such as high power and large driving ability; last, it is difficult to reconcile the contradiction between the long-time stability and fast degradation of transient electronic devices, which greatly limits the reliability of transient electronic devices.

In order to solve the abovementioned problems of transient electronic devices that can degrade and disappear themselves and thus expand their scope of application, in this paper, a destruction mechanism to rapidly crack integrated circuit chip by using instantaneous expansion stress was proposed, which can be applied in the field of information security to reduce the risk of information theft and ensure information security. The conventional package structure was adopted in the scheme, and the energetic material was filled between the chip and the package. The power-on ignition bridge resistance was used to rise temperature rapidly and trigger the cascade reaction of energetic materials to cause gas instantaneous expansion and stress release. The chip cracked under the pressure of gas expansion. This information destruction method can eliminate the unrecoverable information almost instantaneously, which has greatly improved the security of information.

The paper is organized as follows: Section 2 presents a historical perspective of the field. The structure, material, and destruction mechanism of the device are presented in Section 3. The finite element simulation of the structure is carried out to get the appropriate cracking structure in Section 4. The feasibility of the structure and the destruction mechanism are verified by experiments in Section 5. The results of the simulation and experiment are compared and analyzed in Section 6. Finally, outlook and concluding remarks are put forward in Section 7.

## 2. Historical Perspective

In recent years, researchers have done a lot of research studies on the materials, preparation technology, and triggering mechanism of transient electronics. The materials of transient electronic devices can be divided into substrate materials, dielectric materials, interconnection conductor materials, and functional materials. Silk, cellulose, and some high polymer materials have been proved to be suitable for the preparation of transient electronic devices. For example, silk [6] has been used as substrate material and packaging material for a variety of transient electronic devices such as high-performance transistors [5], remote control devices [7], and biodegradable batteries [8]. The degradation rate of the silk can be adjusted from a few minutes to several years by adjusting the crystallinity of the silk. Cellulose is soluble because it contains linear glucose chains [9]. Cellulose and its derivatives have been widely used in printing electronics, paper-based electronics, and nanosensors [10, 11]. Degradable polymers such as polyvinyl alcohol, polyvinylpyrrolidone, polylactic acid, polyglycolic acid, polycaprolactone, and polyhydroxybutyrate are also suitable for use as degradable substrates [6]. The most common

biodegradable dielectric materials include semiconductor materials such as Si [12], Ge [13], and  $\text{Si}_3\text{N}_4$  [13], as well as oxides such as  $\text{SiO}_2$  [14], ZnO [15], MgO [16],  $\text{TiO}_2$  [17], and  $\text{In}_2\text{O}_3$  [18]. Rare earth oxide [19] and nanocomposites [20] have also been proved to be used as dielectric materials for devices. Soluble metals such as Mg, Zn, Fe, W, and Mo can be used to manufacture metal interconnects [13, 21] and bioabsorbable electronic products such as transistors, biomedical implants, and sensors. Liquid metal [22] and nanometal composites [23] have also received extensive attention in addition to solid metal. Functional materials refer to the materials used in electronic components to achieve special functions. PDMS material can be used as a sacrificial layer in transfer printing technology to achieve device transfer [24]. PVA film can be used as the material for substrate, diaphragm, battery packaging, and so on.

At present, the preparation technologies of transient electronic devices mainly include vacuum-based mask deposition, transfer printing, and inkjet printing. In vacuum-based mask deposition, a thin line mask is made by cutting or etching polyimide films and attached to the substrate for selective material deposition. This technology can process many biodegradable electronic materials into functional layers, including Mg [5], Fe [14], ZnO [14], MgO [5], and SiO [5]. However, the use of shadow masks does not allow feature sizes below a few micrometers, resulting in limited resolution of the deposited material. Therefore, vacuum-based mask deposition is not applicable to complex circuits [24]. To address the abovementioned application limitations of vacuum-based mask deposition technology, transfer printing technology emerged as a new alternative. Transfer printing refers to the technology of transferring processed and integrated materials from one substrate to another [25]. The device is prepared temporarily on a conventional substrate such as a silicon wafer by a standard IC process and then transferred to a degradable substrate using a sacrificial layer. It expands the range of machined substrates by isolating the harsh conditions of IC manufacturing processes (such as heating and etching) from the target substrates. Inkjet printing involves two steps: printing and sintering. First, the required graphics and components are printed on the substrate through modern printing technology. Then the printed micro/nanoparticles are tightly bonded together through sintering to maintain electrical continuity and improve electrical conductivity [6]. The sintering process is usually carried out by heating, which is not practical for degradable materials in most cases. In order to avoid thermal damage of printing particles during sintering, local heating methods such as photonic sintering, laser sintering, and other high-energy beams can be adopted [26]. Sintering can also be achieved by electrochemical method at room temperature, which can completely prevent overheating impact [26, 27]. Inkjet printing technology is a promising light manufacturing technology, which can achieve printing at room temperature and pressure and thus greatly reduce the production cost. The technology is suitable for both organic and inorganic materials such as mixed ink, glass, chip, paper, and plastic and can be used as an alternative to standard vacuum deposition and lithography.

How to quickly trigger and efficiently destroy devices is a key research direction of transient electronic technology, and the simplest and earliest studied destruction method is to use wet chemical reaction to dissolve electronic components such as semiconductor, medium, metal, and polymer. The principle is to destruct devices by triggering biodegradable materials through water, acid, light, temperature, and other conditions. Using silk (soluble in water and enzymes) as the substrate and packaging material, Mg as conductor, MgO as dielectric, monocrystalline silicon nanofilm as semiconductor, Suk-Won Hwang produced simple electronic devices including transistors, diodes, inductors, capacitors, and resistors by transfer printing technology [24]. The hydrolyzable materials were used in the circuit diagram, and the whole structure could be disintegrated within 10 min [28]. The hydrolysis process of key materials was recorded. Si nanofilms could be dissolved in poly(butylene succinate) for 12 days, and Mg (150 nm) was completely hydrolyzed in deionized water for 3 h. The MOS device model was prepared by utilizing the expansion property of the substrate (poly lactic-co-glycolic acid) in the process of dissolution. During the hydrolysis of the device, the substrate expansion led to the structural fracture/disintegration of the supporting device, thus accelerating the degradation. Some materials would be degraded under certain conditions. Chan Woo Park prepared mesylate (MSA) and sealed it with wax to obtain the hard silicone wax coating material by acid/wax emulsion fusion casting method [29]. The material coated on the surface of a device would melt and release acid when the temperature reaches a certain level, which would destroy the device quickly. Mg (300 nm) serpentine resistance was prepared on a glass substrate and coated with mesylate wax. The Mg resistance degraded after being heated at 55°C for 2 min. A silicon PIN diode array based on Mg electrodes was fabricated on cyclic poly(phthalaldehyde) (cPPA) substrate using transfer printing technology. Hernandez exposed 2-(4-methoxyphenyl)-4,6-bis (trichloromethyl)-1,3,5-triazine under ultraviolet light to generate highly active Cl, which then absorbed hydrogen from the environment to form hydrochloric acid (HCl) to degrade cPPA polymer rapidly [30]. The degradation rate of the device could be adjusted by changing the irradiance of the UV light source. The samples were damaged within 7 min under the UV intensity of 1.70 MW/cm<sup>2</sup> and within 15 min under the UV intensity of 0.70 MW/cm<sup>2</sup>.

Although transient electronic technology has a lot of achievements in the destruction of devices by degradation, due to the requirement of chemical dissolution, there are few materials to choose from, with limited shape and function of the equipment. The destruction effect of these transient electronic devices largely depends on the dissolution process, but the lack of on-demand control capability limits their application in nonbiological aspects [31]. Li introduced a mechanical failure mode of transient devices [32]. The gate dielectric layer of the MOS tube was composed of SiO<sub>2</sub> (70 nm) and Al<sub>2</sub>O<sub>3</sub> (13 nm), the source, drain, and gate electrodes were composed of Cr/Au (5/100 nm), and the polyimide film (12.5 μm) flexible material was used as the

device substrate. A poly- $\alpha$ -methylstyrene (PAMS) intermediate layer was introduced between MOS substrate and electrode. PAMS layer is a kind of high-performance resin, which will be decomposed into gaseous monomer when heated above a certain temperature, making the device lose support and causing irreversible damage. The device can be destroyed within 3 min through this heat-induced transient behavior. At the initial stage of PAMS degradation, polymer chain fracture is initiated by heat, and a small amount of volatile reduces the electronic properties of Si-nano-membrane (SI-nm) resistance. When the critical failure temperature (300°C) is reached, a large amount of gas accumulates below SI-nm, and the accompanying high pressure causes the device breakdown. Gao [31] used poly( $\epsilon$ -caprolactone) (PCL) nanofiber film as the substrate to fabricate optical detection array and Si film on PCL by transfer printing technology. Due to the relaxation and porosity of the nanofibers' microscopic polymer chains, the nanofibers' pores collapse under heating conditions, resulting in a 97% reduction in PCL volume. The device collapses under the heating condition of 90°C within 2 s, leading to the function failure. By integrating a thin resistance heater as the source of the Joule heating trigger, the controlled destruction of the device is achieved. Lee et al. [33] and Gumus et al. [34] used similar methods. A layer of expandable polymer is added between the flexible substrate and the silicon film. Pandey [35] mixes gasoline, benzene, polystyrene, and CuO/Al nanoparticles to form a napalm film and assembles it onto a chip. The chip melts by burning the napalm for about 10 s. Chen et al. [36] present an electrochemically triggered transience mechanism of Si by lithiation, allowing complete and controllable destruction of Si devices, which can lead to both physical disintegration and chemical modification of the Si component that could completely eliminate potential device recovery.

Although the research on triggering mechanism and degradation mode of transient devices has achieved some progress, there is no mature technology to realize controllable triggering and rapid destruction on demand, with a certain gap from the real transient. The degradation rate of degradation devices is not up to the requirement of practical application, and the limitation of triggering mode also restricts the application of transient devices.

### 3. Structure, Materials, and Destruction Mechanisms

Based on the traditional dual inline-pin package, the bottom of the chip was grooved and filled with energetic material. The ignition bridge was sandwiched between the chip and the package shell and contacted the energetic material. Both ends of the ignition bridge were connected to the pins by leads to achieve external current control. The energetic materials were heated and expanded to damage the chip when the ignition bridge was powered on. The cracking structure profile is shown in Figure 1.

The instantaneous chip cracking structure was considered with the compatibility of trigger mode, material, and encapsulation process. The traditional materials and

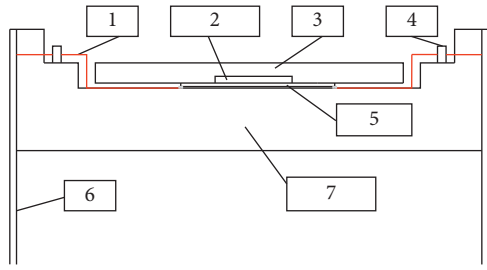


FIGURE 1: Schematic diagram of the package structure profile. (1) Lead; (2) energetic material; (3) chip; (4) tube base; (5) ignition bridge; (6) pin; (7) ceramic package shell.

packaging were used as much as possible to reduce problems in processing and use. The substrate and the device were made of traditional monocrystalline silicon that was the best material choice because many problems of instantaneous degradation materials have not been solved. The ignition bridge was made of NiCr alloy film because of its stable performance, high resistivity, excellent heating effect, strong adhesion, and easy preparation, and it can be directly integrated with silicon [37]. It can produce instantaneous high temperature above  $600^{\circ}\text{C}$  after it was powered on to provide initial conditions for the cascade reaction of energetic materials. The energetic material was composed of CuO and Al particles with diameters of  $5\sim 10\text{ }\mu\text{m}$  in 2:1 ratio. Common packaging materials include metals, ceramics, and plastics. The package shell was made of ceramics that can withstand high temperature with lower thermal conductivity than metals, which contributed to the instantaneous high temperature inside the package shell and the transient failure of the chip [38].

#### 4. Finite Element Simulation Analysis

The Materials and Methods section should contain sufficient detail so that all procedures can be repeated. It may be divided into headed sections if several methods are described. A simplified finite element simulation model was built using CAD software based on Figure 1. In order to observe the internal temperature and stress of the structure, a simulation model was established with half of the actual structure. The complete model was simulated by symmetrical design in the process of ANSYS simulation. At first, the optimum cracking structure was obtained by simulating the minimum cracking temperature for the chips with different shapes and sizes of the groove on the back. Then, the electrothermal and static structural coupling simulation analysis was conducted to predict the cracking effect of the structure after the proper structure was selected.

**4.1. Transient Dynamics Simulation.** The slotting mode of the chip was determined by using the transient dynamics analysis module in ANSYS preliminarily. The model of transient dynamic analysis was composed of the upper chip and ceramic shell combined and the middle groove filled with energetic material, as shown in Figure 2. The stress of the chip was simulated by applying temperature to the

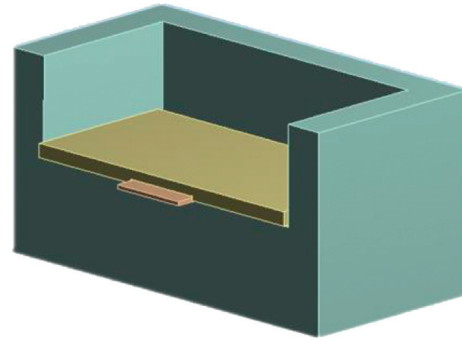


FIGURE 2: Model of transient dynamic analysis.

energetic material in the groove, and then, the critical temperature of chip cracking was obtained by changing the temperature iteration simulation. The chip failure condition was defined as the tensile strength of silicon reached  $3.5 \times 10^8\text{ Pa}$  [39] when the chip cross section had a complete penetrating part.

The mechanical parameters of the materials in the transient dynamic analysis are shown in Table 1. The thermite reaction occurred when the thermite was heated to the temperature that can trigger reaction [40], releasing  $4.05 \times 10^5\text{ J/mol}$  [41] and producing a great impact force in a confined space. In the simulation, the expansion material with a large expansion coefficient [42] was used as a reference because it was difficult to measure the expansion coefficient of the thermite used.

The chip was  $350\text{ }\mu\text{m}$  thick and covered an area of  $8\text{ mm} \times 8\text{ mm}$  in the simulation model. By changing the shapes and sizes of the groove in the model, the appropriate structure was selected to prepare for the subsequently integrated simulation. The simple structure of transient dynamic analysis was conducive to faster changing the model structure and reducing the time of subsequent electro-thermal coupling iterative simulation after the shape and size of the groove were selected. For the transient dynamic simulation, the round and square grooves with sizes of  $1\text{ mm}^2$ ,  $4\text{ mm}^2$ ,  $9\text{ mm}^2$ , and  $16\text{ mm}^2$  and depths of  $25\text{ }\mu\text{m}$ ,  $50\text{ }\mu\text{m}$ ,  $75\text{ }\mu\text{m}$ , and  $100\text{ }\mu\text{m}$ , respectively, were selected. The models of different sizes were simulated, respectively. The temperature is the independent variable, and the maximum stress on the silicon wafer is the dependent variable. The stress on the silicon wafer was obtained by simulation. The dichotomy was used to narrow the temperature range under the premise that the stress on the silicon wafer was greater than and closest to  $3.5 \times 10^8\text{ Pa}$ . The temperature with an error of less than  $10^{\circ}\text{C}$  is considered as the minimum temperature required for chip cracking. The minimum cracking temperature was used to judge the cracking effect of different grooves. The lower the temperature required for structural cracking was, the more likely the structure was to crack. The temperature simulation results of ANSYS dynamics are shown in Figure 3. The structural stress distribution under different grooves is shown in Figure 4.

The following results can be obtained from Figure 3. The temperature required to destroy the chip of the circular groove structure was slightly lower than that of the square



TABLE 1: Mechanical parameter of material.

Materials	Density ( $\text{g cm}^{-3}$ )	Young modulus (GPa)	Poisson's ratio	Expansion coefficient ( $^{\circ}\text{C}^{-1}$ )
Ceramics	3.96	400	0.233	$5 \times 10^{-5}$
Expansion material	2.56	531	0.294	
Silicon	2.33	169	0.28	
Ignition bridge	8.4	10	0.3	

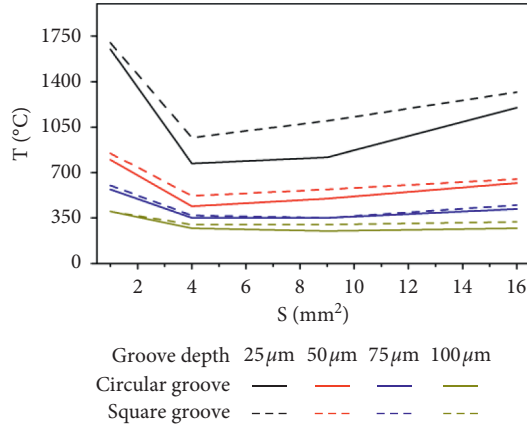


FIGURE 3: Temperature of the chip is cracked under different groove conditions.

groove structure when the heights and surface areas of the grooves were the same. But shape was not the main factor affecting the cracking effect. The temperature decreased with the increase of groove depth when the shapes and surface areas of grooves were the same. Different depths had an obvious influence on the cracking effect. The temperature decreased first and then increased with the increase of groove area.

The temperature decreased due to the expansion force gathering in the center breakthrough, and the increase in the volume of the expansion material resulted in a better cracking effect when the groove area was small. However, when the groove area increased to a certain extent, the surface of the expanding material expanded more evenly, the stress concentrated more obviously at the edge of the groove, which dispersed part of the expansion force, and thus, the chip would crack at higher temperatures.

A circular groove with an area of  $1 \text{ mm}^2$  and a depth of  $0.1 \text{ mm}$  was etched on the back of the chip for electrothermal and static structural coupling simulation, considering the effect of heating during processing and use.

**4.2. Electrothermal and Static Structural Coupling Simulation Analysis.** Firstly, the temperature of the power-on structure was simulated by electrothermal coupling. Then, the temperature result was taken as the input condition of the static simulation to simulate and analyze the stress of the structure. The simulation model is shown in Figure 5. The electrothermal simulation found that a lot of heat was absorbed by ceramics due to the high thermal conductivity of the materials. A thermal insulation layer was added between the ignition bridge and the ceramics to reduce heat loss.

The simulation results of thermal insulation effects of thermal insulation layers with different thicknesses are shown in Table 2. When the heat insulation layer thickness was  $0.1 \text{ mm}$ , the maximum temperature of the model was  $1503^{\circ}\text{C}$ . Combined with the melting temperature of NiCr resistance, it could be concluded that the thermal insulation effect was already very good. Therefore, the thermal insulation layer thickness was set as  $0.1 \text{ mm}$ .

The ignition bridge was made of NiCr alloy thin film with a size of  $840 \mu\text{m} \times 80 \mu\text{m} \times 6 \mu\text{m}$  and a resistance of  $2 \text{ ohms}$ . The experimental results showed that the ignition bridge would fuse within  $60 \text{ ms}$  at the current of  $0.5 \text{ A}$  in the air. Therefore, the current applied to the ignition bridge of the symmetric model was  $0.25 \text{ A}$ , the air convection heat coefficient was defined as  $10 \text{ W/m}^2 \cdot ^{\circ}\text{C}$ , the action time was  $50 \text{ ms}$ , and the initial temperature was  $25^{\circ}\text{C}$ . Thermophysical parameters of the materials in the electrothermal coupling simulation are shown in Table 3.

The temperature distribution of the cracking structure was analyzed by electrothermal coupling simulation, as shown in Figure 6. The results showed that the maximum temperature in the center reached  $1503^{\circ}\text{C}$ , and the overall temperature of the expansive material was higher than  $700^{\circ}\text{C}$ .

The temperature distribution of the electrothermal coupling simulation was taken as the input condition of statics simulation to set the mechanical parameters of the materials in the structure and simulate the structure. The mechanical property parameters of materials in the static simulation are shown in Table 1. The pressure distribution of the final ANSYS simulation results is shown in Figure 7. The yellow part (pressure greater than  $3.5 \times 10^8 \text{ Pa}$ ) runs through the chip cross section, indicating that the chip can be destroyed.

## 5. Experimental Verification

**5.1. Preparation of Test Sample.** The author prepared a sample with reference to simulation results. (1) Chip preparation: a wafer with memory function was purchased and a circular groove with an area of  $1 \text{ mm}^2$  and a depth of  $0.1 \text{ mm}$  was etched on the back of the wafer by dry etching. The chip to be tested ( $3 \text{ mm} \times 4 \text{ mm}$ ) was cut from the wafer by DISCO chip machine and was cleaned with deionized water for  $10 \text{ min}$  and then treated with ethanol for  $5 \text{ min}$ . Thermite was filled into a groove on the back of the chip and cured with ethanol. (2) Built-in ignition bridge: DIP12 ceramic tube shell was used for packaging. The packaging was cleaned with ultrasonic acetone for  $5 \text{ min}$  and then cleaned with ethanol for  $5 \text{ min}$ . The purchased ignition bridge ( $840 \mu\text{m} \times 80 \mu\text{m} \times 6 \mu\text{m}$ ) was fixed to the shell using

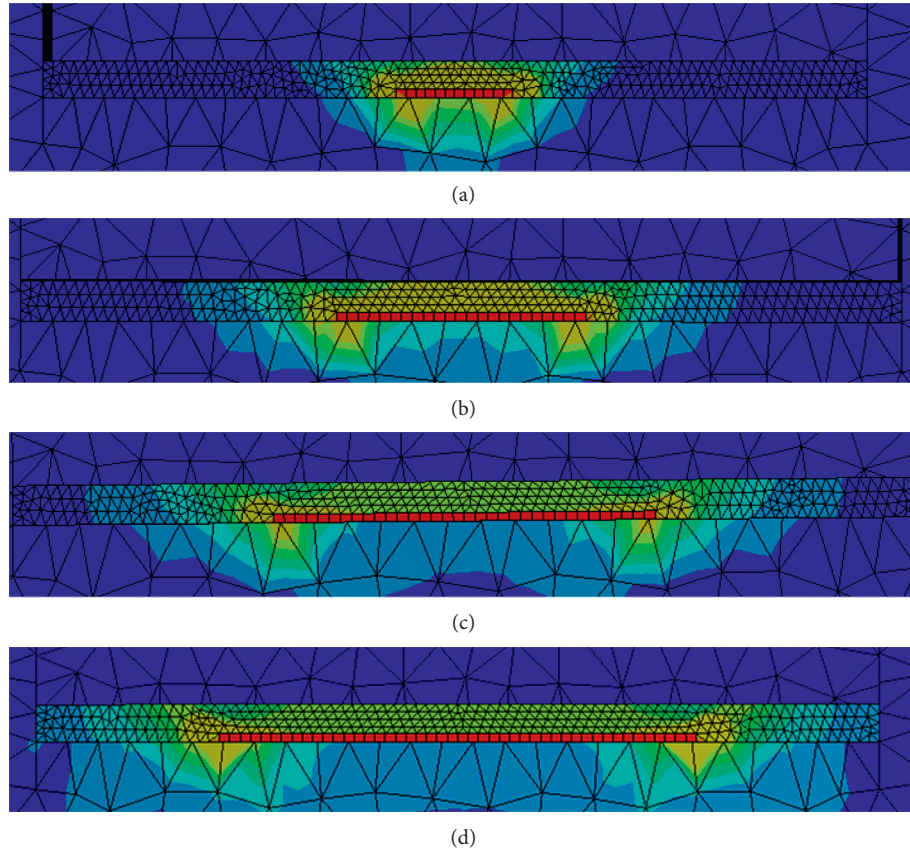


FIGURE 4: Comparison of stress concentration under different groove conditions: (a) 1 mm<sup>2</sup>, (b) 4 mm<sup>2</sup>, (c) 9 mm<sup>2</sup>, and (d) 16 mm<sup>2</sup>.

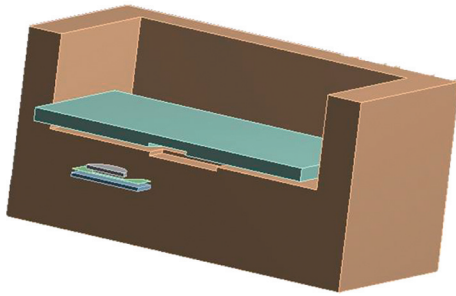


FIGURE 5: The model of electrothermal and static coupling simulation.

TABLE 2: Temperature variation under different heat insulation thickness.

Heat insulation thickness (mm)	0.05	0.1	0.15
Temperature (°C)	1250	1503	1680

A-400-36 insulating gel. Both ends of the ignition bridge and the packaging pins were welded manually using a tinned copper wire with a diameter of 210  $\mu\text{m}$ . (3) Chip encapsulation: the chip was pasted onto the shell using the existing H20E conductive adhesive. Then, the connection points on the chip were bonded with the pins using a gold wire with a diameter of 25  $\mu\text{m}$ . Finally, the cover plate was fixed on the upper part of the shell with adhesive tape to

protect the chip. The chip after slotted and the experimental sample prepared are shown in Figure 8.

**5.2. Test System Setup.** A test verification system was built in order to obtain the cracking time and the cracking effect accurately. The system consisted of a digital storage oscilloscope (KEYSIGHT MSOX4104A), a computer, a test board, and a power supply (DPS-500AB-32A). The test board was integrated with MCU (STM32F303) and memory chip DUT to be tested, as well as memory chip EEPROM (BL24C256A) and regulator chip (TPS74401RGWT) for comparison.

The connection relationship of each part is shown in Figure 9. The computer, oscilloscope, contrast memory, and memory to be tested were connected to the single-chip microcomputer of the test board, respectively. The power supply converted the 5 V input voltage to 3.3 V through the voltage regulator chip to meet the operating voltage of the system. The comparison memory chips were used to check whether the system was working properly and to compare with the experimental samples to be tested. The computer was used to verify whether the memory DUT's read-write function failed. The oscilloscope was used to measure the time of chip failure.

**5.3. Experimental Results.** Before the chip cracked, DUT worked normally, oscilloscope waveform always switched between high and low levels, and the computer read and wrote

TABLE 3: Material electrothermal physical parameters.

Materials	Resistivity ( $\Omega \cdot m$ )	Specific heat capacity ( $J \cdot (kg \cdot ^\circ C)^{-1}$ )	Heat conductivity coefficient ( $W \cdot (m \cdot K)^{-1}$ )
Ceramics	10.15	820	18
Expansion material	10	800	0.27
Heat insulation thickness	1015	1.09	0.05
Ignition bridge	$1.15 \times 10^{-6}$	0.44	12.171
Silicon	2	703	0.21

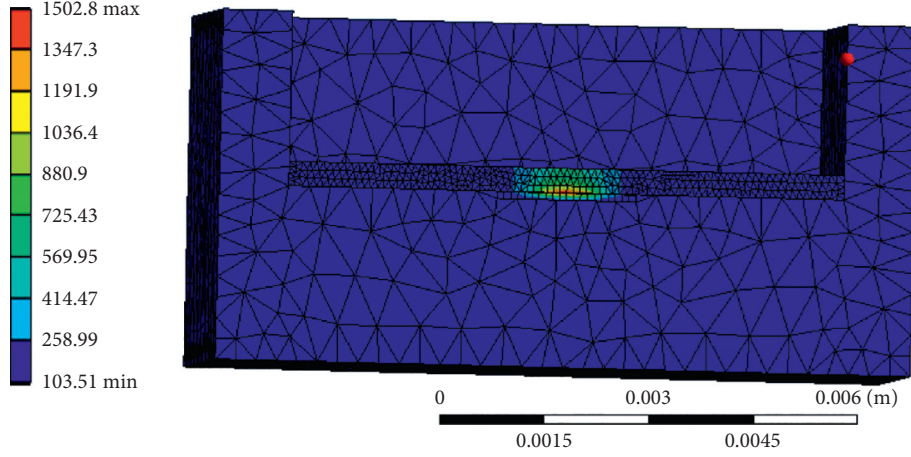


FIGURE 6: Temperature distribution of electrothermal simulation.

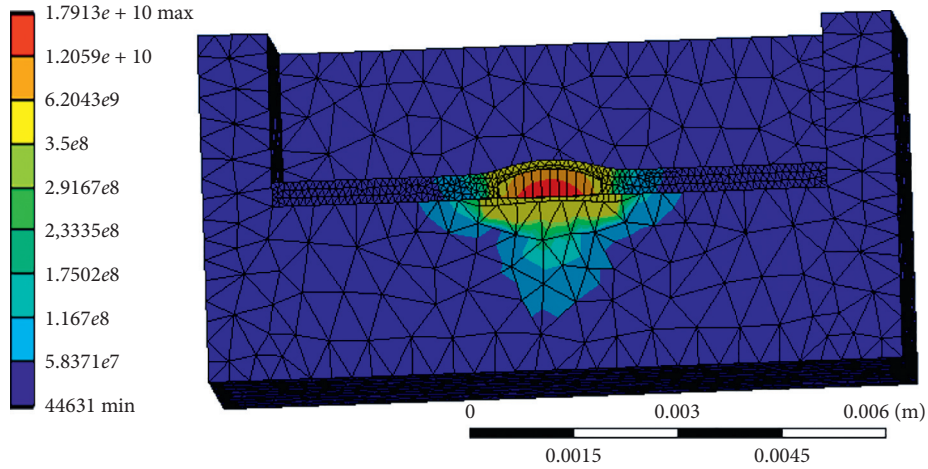


FIGURE 7: Pressure distribution of static simulation analysis.

data to memory normally. The chip cracking experiment was carried out by applying 5 V voltage to the pins connected to the ignition bridge. The shell made a sharp sound with a slight spark almost immediately when the switch was turned on. After the chip cracked, the shell cover plate was bent outward under the impact force released from inside. The appearance of the cracked chip is shown in Figure 10. The chip cracked under high pressure caused by the expansion of the thermite reaction and was burned to some extent.

The experiment achieved the destruction of the chip at the physical level. The variation of input voltage of power and output voltage of memory with time during the experiment is shown in Figure 11. The voltage gradually

increases from 0 V after the power switch is turned on and stabilizes at 5 V after about 25 ms. The output of the memory can vary between high level and low level (3.3 V and 0 V) during the initial phase of power on. The output value of the memory is out of order and cannot enter the low level again after powered on for about 6.1 ms. Subsequently, it maintains at high levels (the high level is less than 3.3 V under the influence of the circuit). The power input voltage is 2.175 V at this point. The read-write test of the memory is shown in Figure 12. The read-write memory failed after the chip cracked. The experimental results have shown that the cracking structure can enable the chip to fast crack and fail by the external current effectively.



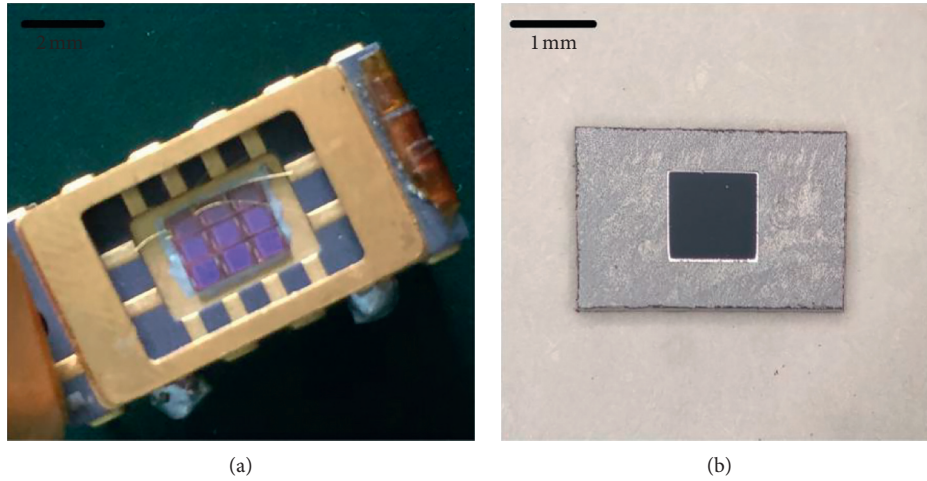


FIGURE 8: (a) Chip after slotted. (b) Sample of the finished package.

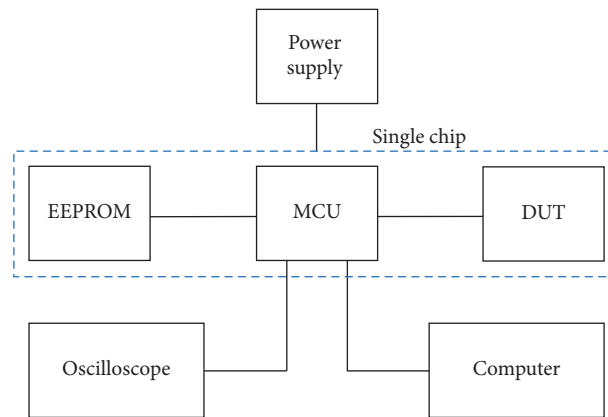


FIGURE 9: Composition of the test system.

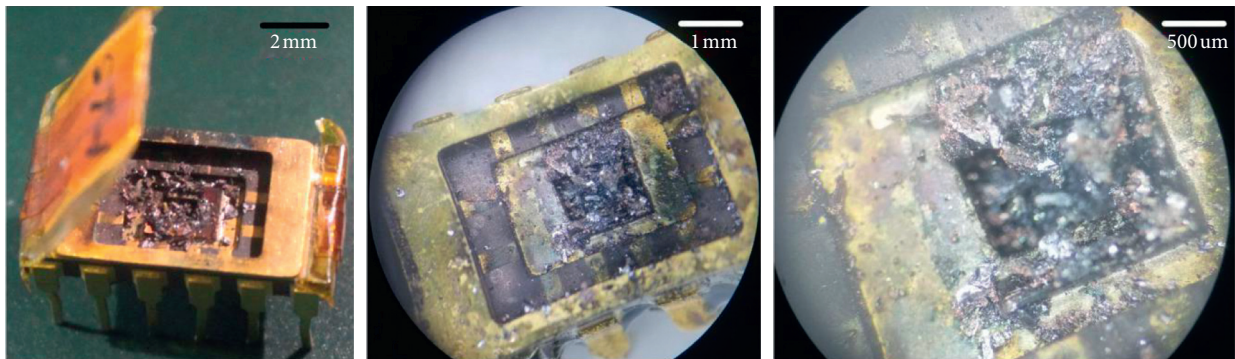


FIGURE 10: Appearance of the cracked chip.

## 6. Discussion

In the simulation, a thermal insulation layer was added to reduce the influence of ceramic heat dissipation, so as to better reflect the simulation effect. In the experiment, there was a gap between the ignition bridge and the shell actually, so heat dissipation could be ignored. Moreover, the

expansion effect of energetic material was better than that of expansive material. The time of triggering crack was short, so the cracking effect was not affected even without the thermal insulation layer. The experimental results have shown that the chip cracking was triggered at the current of 1 A and at 6.1 ms, while the current was 0.5 A and the time was 50 ms in the simulation. The main reason was that the filling materials



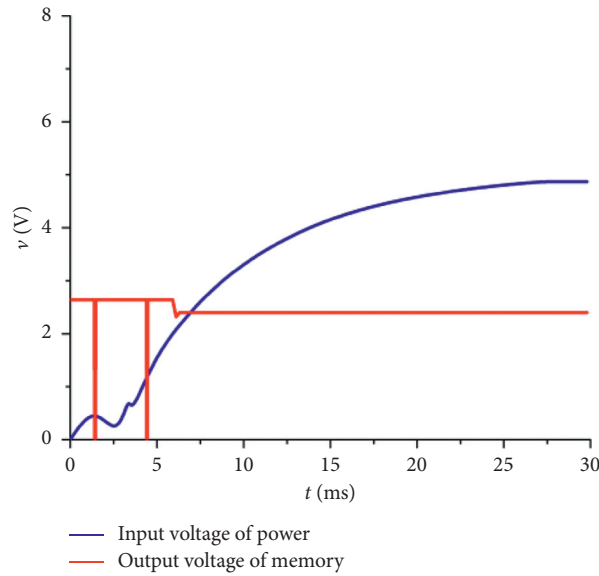


FIGURE 11: Changes of power input voltage and memory output level.

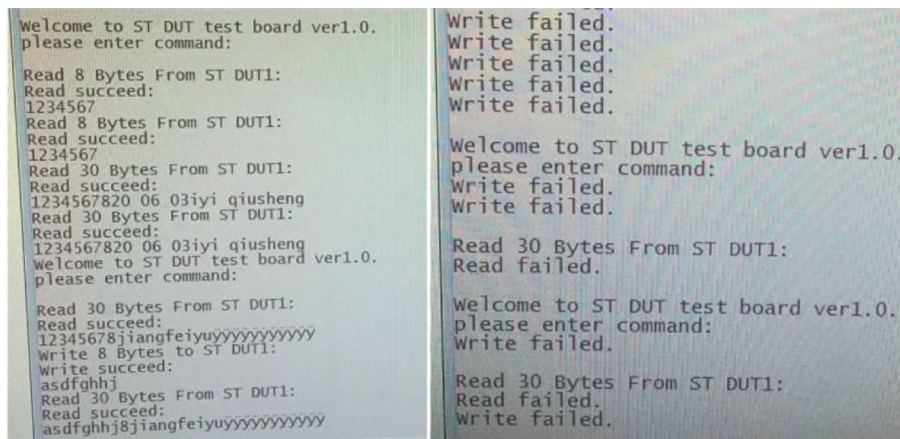


FIGURE 12: Changes of memory function of read-write before and after the experiment.

were different for the simulation and experiment. Thermite was triggered quickly at a current of 1 A to achieve chip cracking, while expansion material was heated continuously for a relatively long time at a current of 0.5 A to realize chip cracking. The simulation and experiment have shown that the cracking structure is feasible to ensure information security by destroying the chip quickly.

The structure designed in this paper can cause the physical destruction of electronic devices at the chip level and make the chip fail quickly. Compared with the quick erasure and encryption algorithm, the designed method is safer in recoverability and can solve the problems of adaptive scene limitation and slow degradation rate of degradation devices. Due to the limitation of experimental conditions, it is difficult to measure the expansion coefficient of thermite, so the ANSYS simulation data are not completely consistent with the actual experimental results in the cracking time and cracking effect. But the simulation provides a good reference for the selection of shapes and sizes of grooves in

the experiment. At present, the experimental system designed has set a trigger switch, which needs to be manually controlled. In the future, remote control triggering and inductive automatic triggering should also be studied, so as to achieve self-destruction when the security chip is threatened.

## 7. Conclusions and Outlook

A review of recent progress on studies related to materials, process technology, and destruction mechanism of transient electronic devices is presented in this paper. The focus of the paper was to analyze the triggering mechanism and destruction mode of transient electronic devices. The structure and destruction mechanism of a transient electronic device are presented and analyzed by ANSYS finite element simulation software. The sample was prepared and a test system was built to verify the feasibility of the structure. The finite element analysis of ANSYS has shown that the depth of the

groove was the main factor affecting the cracking effect. The chip cracking effect was improved with the increase of groove depth. The shape of the groove had little effect on the cracking effect. The chip cracked within 50 ms at the trigger of current of 0.5 A when a circular groove with an area of 1 mm<sup>2</sup> and a depth of 0.1 mm was filled with an expansion material with an expansion coefficient of 10<sup>-5</sup>.°C<sup>-1</sup>. The sample was prepared for the cracking experiment, and the chip cracked and failed within 10 ms at a current of 1 A. Both simulation and experiment have shown that the structure and destruction mechanism can achieve the fast destruction of the chip, ensure the information security, and solve the security problem that the core information may be stolen.

Transient electronic technology has made great progress in materials, processing technology, destruction mechanism, and other aspects, which has promoted its development and improved the theoretical system. However, the development of transient electronic technology is still in the initial stage. Due to the limitation of materials, the slow destruction speed of devices, trigger mechanism, preparation process, and device performance need to be improved. These problems limit the application scope of transient electronic devices. With the continuous improvement of new materials, processing technology, and destruction mechanism, transient electronic devices have a broad application prospect in high-end equipment, in addition to environmental, medical, and other fields. Transient electronic technology will develop towards material diversification, simple triggering mode, economic production, and high integration of devices.

## Data Availability

The data used to support the findings of this study are included within the article.

## Conflicts of Interest

The authors declare that there are no conflicts of interest regarding the publication of this paper.

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