

Research Article

An Ameliorated Small-Signal Model Parameter Extraction Method for GaN HEMTs up to 110 GHz with Short-Test Structure

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An improved method of extracting small-signal equivalent circuit model parameters for gallium nitride high electron mobility transistors (GaN HEMTs) is presented. This paper intends to present a method to extract the parasitic inductance and resistance of transistors based on the short-test structure without the open-circuit test structure. The parasitic capacitance of transistors is extracted by the method based on the size scalable model. Compared with the traditional COLD-FET method, the extraction procedure is simpler and more convenient. After removing the influence of parasitic elements, the intrinsic parameters of the model can be extracted by the S -parameters measured at different bias points. The experimental results show that the simulation results have good agreement with the measured results in the range of 0.5~110 GHz.

1. Introduction

GaN high electron mobility transistors have been widely applied in high power and high frequency applications due to their high breakdown voltage and high electron saturation rate [1]. In order to better reduce the cost and shorten the design time in the process of integrated circuit design, it is essential to establish an accurate small-signal circuit model that can work in the RF and microwave frequency band [2–5]. Moreover, the accuracy of the S -parameter of the device under test is of great significance to the small-signal model, and it is necessary to obtain the accurate S -parameter of the device under test. When conducting S -parameter measurements of the microwave device directly on a wafer, the parasitic effect of metal lines and PAD cannot be ignored. Therefore, considering the parasitic effect of test structure can better improve the accuracy of the model.

It is very obvious that once the parameters of the parasitic elements are determined, the intrinsic elements can be directly obtained after de-embedding the effect of the parasitic elements. Up to now, there have been various methods to extract parasitic elements based on scattering parameter measurement. In the traditional method [6], the pad capacitance can be extracted by

using the open-test structure [7]. However, this method requires a special test structure for each device size on the wafer, and the inhomogeneity on the wafer must be ignored. In this paper, the equivalent circuit parameters of the test structure are determined [8]. Four GaN HEMTs with different sizes but identical test structures were used to extract the parasitic capacitance. Through the above method, the open-test structures can be ignored and the extraction of parasitic parameters is simplified. In this paper, the scalable small-signal model for GaN HEMTs devices has been developed. An improved extrinsic elements extraction procedure has been proposed. The main contribution of this paper is that the scalable rules for the small-signal model up to 110 GHz are given in detail. Compared with traditional methods [9–11], the proposed method has presented an update of the classical small-signal parameter extraction method, which is very valuable for the industry. Because the use of this method implies that open structures are not necessary. Advantages are clear in terms of area saving, characterization, and data analysis time.

The organization of this paper is as follows. In Section 2, the small-signal equivalent circuit model used in this paper is introduced. In Section 3, the improved method of extracting

parasitic and intrinsic parameters is introduced, and the parameters of the device are extracted by the test structure. In Section 4, the simulation results are compared with the measurement results.

2. Small-Signal Equivalent Circuit Model of GaN HEMT

Five different GaN HEMTs are adopted in this study; they are TZ0210, TZ0420, TZ0630, TZ0840, and TZ0860. All of them were manufactured by UMS using GH15-10 process with 150 nm gate length. The gate width of TZ0210 is 10 μm and the number of fingers is 2; the gate width of TZ0420 is 20 μm and the number of fingers is 4; the gate width of TZ0630 is 30 μm and the number of fingers is 6; the gate width of TZ0840 is 40 μm and the number of fingers is 8; the gate width of TZ0860 is 60 μm and the number of fingers is 8. The above devices are based on GaN-on-SiC process.

The two-port S-parameter has been measured in the frequency range from 500 MHz to 110 GHz. The de-embedding method based on short-test structure has been performed to remove the parasitic component of the PADs and interconnect lines.

Figure 1 shows the equivalent circuit of the GaN HEMT. The model consists of two parts: the parasitic elements independent of bias voltage and the intrinsic elements dependent on bias voltage. C_{pg} and C_{pd} represent the PAD capacitance of the gate and drain between the signal PAD and the ground, respectively. C_{pgd} represents the coupling capacitance between the gate and drain PADs. L_g , L_s , and L_d represent the inductance of the gate, source, and drain interconnecting lines, respectively. R_g , R_s , and R_d represent the resistance of the gate, source, and drain interconnecting line, respectively. C_{gs} , C_{gd} , and C_{ds} are the gate-source, gate drain, and source drain intrinsic capacitance, respectively. R_i is the intrinsic channel resistance, g_m is the transconductance, g_{ds} is the drain output conductance, and τ is the time delay. R_{pg} and R_{pd} , respectively, represent substrate losses of input PAD and output PAD.

3. Parameter Extraction and Results and Discussion

The resistance and inductance values of the interconnecting lines and the capacitance values of PADs can be determined by testing the S-parameters of the HEMT device's short-test structure. The value of the intrinsic element can be calculated after removing the influence of the parasitic element.

3.1. Extraction Methods of Parasitic Element. When the active device works in the cutoff region, it presents capacitive passive network characteristics, so the PAD capacitance can be extracted by using the S-parameter and admittance parameter of low frequency (0~10 GHz) measured under the cutoff condition. However, a common premise of these methods is the assumption that the gate-source and drain-

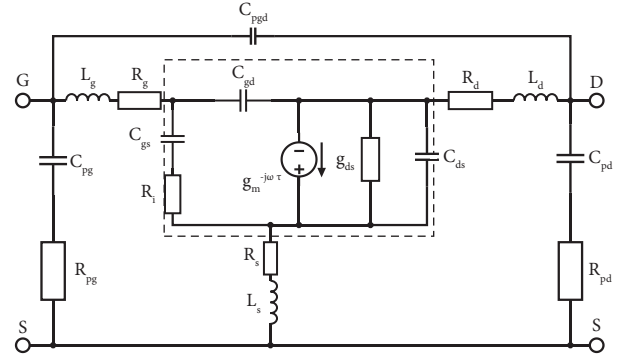


FIGURE 1: The equivalent circuit model of the GaN HEMT.

source capacitance of all symmetric FETs is equal in the COLD-FET bias case, so the application range of this method is limited. This paper presents a parasitic capacitance extraction method based on the proportional model, which can effectively overcome the above disadvantages.

The formula of the traditional COLD-FET method to extract parasitic is as follows:

$$\begin{aligned} C_{pg} &= \frac{\text{Im}(Y_{11})}{\omega} - C_{pgd}, \\ C_{pg} &= \frac{\text{Im}(Y_{22})}{\omega} - C_{pgd}, \\ C_{pgd} &= -\frac{\text{Im}(Y_{12})}{\omega}. \end{aligned} \quad (1)$$

The results of parasitic capacitance are shown in Figure 2.

It can be seen from the extraction results in the figure that the values of the parasitic capacitances based on the COLD-FET method are large. The main reason is the influence of the feed lines and transitions between the PADs and feed lines. This problem has been taken into account by the method based on the size scalable model and neglected by the COLD-FET method [12].

The method based on the size scalable model steps is as follows. Firstly, the S-parameter of different gate width devices under the cutoff condition is measured. Secondly, the S-parameter is converted into the Y-parameter (admittance parameter). Finally, the values of the parasitic capacitances are obtained from the imaginary part of the Y-parameter (admittance parameter) [13].

The admittance matrix of Y-parameter is represented as follows:

$$Y = \begin{bmatrix} \frac{j\omega C_{pg}}{1 + j\omega C_{pg} R_{pg}} + j\omega C_{pgd} & -j\omega C_{pgd} \\ -j\omega C_{pgd} & \frac{j\omega C_{pd}}{1 + j\omega C_{pd} R_{pd}} + j\omega C_{pgd} \end{bmatrix}. \quad (2)$$

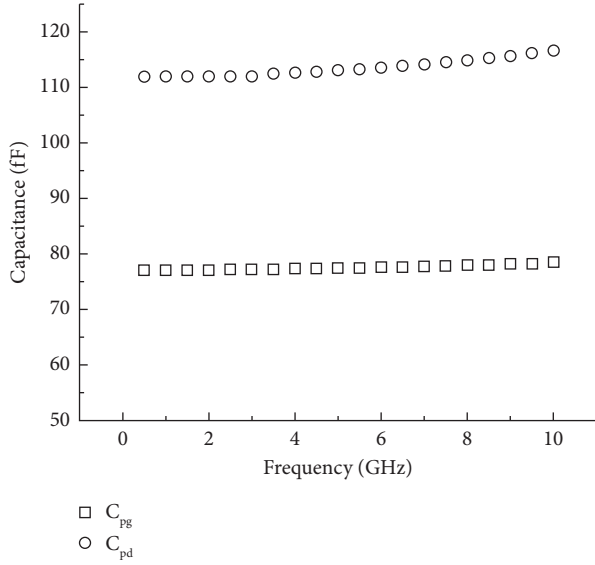


FIGURE 2: Capacitance extraction result of COLD-FET method.

The formula of the equal scalable model method is as follows:

$$\begin{aligned}
 C_{pg} &= \frac{\text{Im}(Y_{11})}{\omega} |_{\omega \rightarrow 0} - C_{pgd}, \\
 C_{pd} &= \frac{\text{Im}(Y_{22})}{\omega} |_{\omega \rightarrow 0} - C_{pgd}, \\
 C_{pg} &= \frac{\text{Im}(Y_{12})}{\omega} |_{\omega \rightarrow 0}.
 \end{aligned} \quad (3)$$

Through the measured S-parameter and Y-parameter of five different devices under the cutoff condition, the mean value of the low frequency (0.5~10 GHz) range was taken as the final value.

The relationship between parasitic capacitance and gate width is shown in Figure 3.

In the fitting function of the relation between the gate width (the GaN PHEMTs with $2 \times 10 \mu\text{m}$, $4 \times 20 \mu\text{m}$, $6 \times 30 \mu\text{m}$, $8 \times 40 \mu\text{m}$, and $8 \times 60 \mu\text{m}$) and the imaginary part of the Y parameter (admittance parameter) in the Figure 3, which shows the relationship between the imaginary parts of the Y-parameters, ($i, j = 1, 2$) and the gate width of the HEMTs. Since the value of C_{pgd} is so small that it is almost negligible, the intercept value can be considered to be the value of C_{pd} and C_{pg} .

Comparing the results of the two methods, it is obvious that the capacitance value obtained by the proposed method is closer to the final optimization result than that obtained by the traditional method.

The values of the substrate resistances can be extracted by the following formulas:

$$R_{pg} = \text{Re}\left(\frac{1}{Y_{11} + Y_{12}}\right), \quad (4)$$

$$R_{pd} = \text{Re}\left(\frac{1}{Y_{22} + Y_{12}}\right). \quad (5)$$

Substrate effects start to be dominant above 50 GHz. Considering the frequency range of this work, which achieves 110 GHz, the substrate resistance value can be extracted using the real part of Y-parameter under high frequency (60~70 GHz) conditions. The results of substrate resistances are shown in Figure 4.

3.2. *Extraction Methods of Parasitic Inductance and Resistance.* The values of the parasitic inductance and the parasitic resistance can be obtained by the following formula:

$$Y^{\text{short1}} = Y^{\text{short}} - Y^{\text{PAD}}, \quad (6)$$

where Y^{short} is the admittance matrix obtained from conversion of the measured S-parameters of the short-test structure (as shown in Figure 5); Y^{short1} is the admittance parameter of the dashed box part of Figure 5 equivalent circuit; Y^{PAD} is the admittance matrix obtained from conversion of the measured S-parameters of Figure 6.

$$Z^{\text{short1}} = \begin{bmatrix} R_g + j\omega L_g + R_s + j\omega L_s & R_s + j\omega L_s \\ R_s + j\omega L_s & R_d + j\omega L_d + R_s + j\omega L_s \end{bmatrix}, \quad (7)$$

where Z^{short1} is the impedance parameter matrix obtained from the conversion of Y^{short1} . Then, we can get the expressions of R_s , R_g , R_d , L_s , L_g , and L_d as follows:

$$\begin{aligned}
 R_g &= \text{Re}(Z_{11}^{\text{short1}} - Z_{12}^{\text{short1}}), \\
 R_d &= \text{Re}(Z_{22}^{\text{short1}} - Z_{12}^{\text{short1}}), \\
 R_s &= \text{Re}(Z_{12}^{\text{short1}}),
 \end{aligned} \quad (8)$$

$$L_g = \frac{\text{Im}(Z_{11}^{\text{short1}} - Z_{12}^{\text{short1}})}{\omega},$$

$$L_d = \frac{\text{Im}(Z_{22}^{\text{short1}} - Z_{12}^{\text{short1}})}{\omega},$$

$$L_s = \frac{\text{Im}(Z_{12}^{\text{short1}})}{\omega}. \quad (9)$$

Finally, the values of the obtained parasitic elements are taken as the initial value for iterative optimization. The optimization results are shown in Table 1.

3.3. *Extraction Methods of Intrinsic Element.* When the operating frequency is relatively low, the effect of the parasitic resistance and the parasitic inductance of the interconnect is almost negligible. However, when the working frequency increases, especially when the working frequency enters the millimeter band, the parasitic inductance of interconnect on the device cannot be ignored, so when the working frequency is high, it must de-embed, and the specific de-embedding process is as follows:

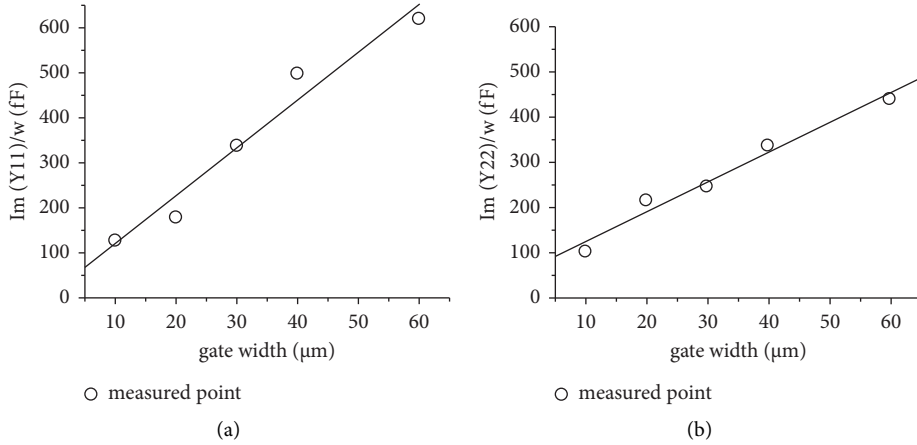


FIGURE 3: Extraction result of equal scalable model method: (a) $C_{pg} + C_{pgd}$; (b) $C_{pd} + C_{pgd}$.

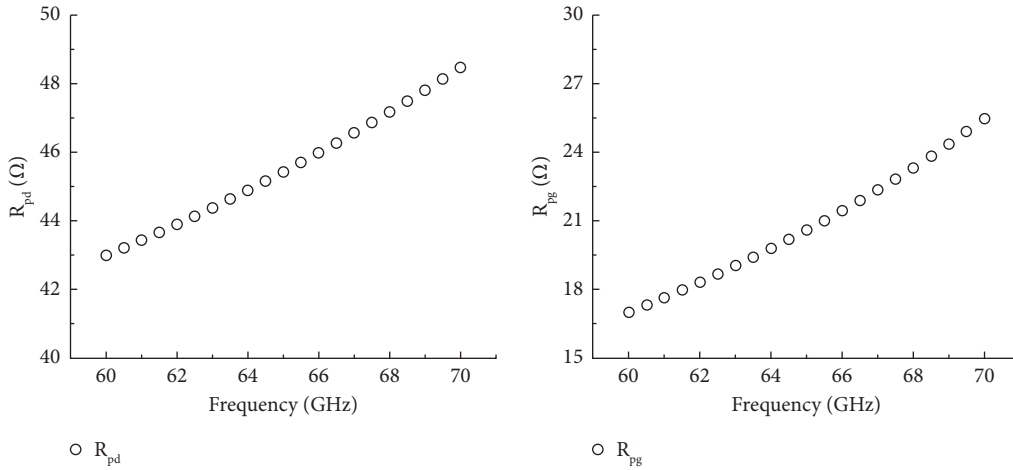


FIGURE 4: Extraction result of substrate resistance.

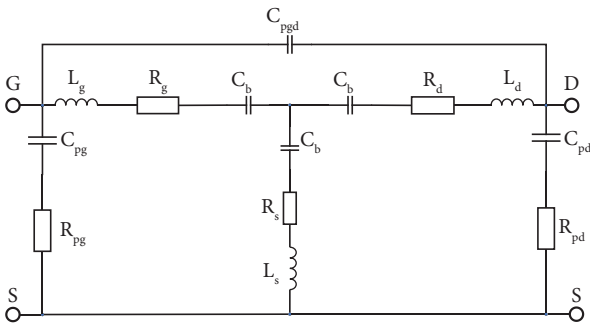


FIGURE 5: The equivalent circuit of the short-test structure.

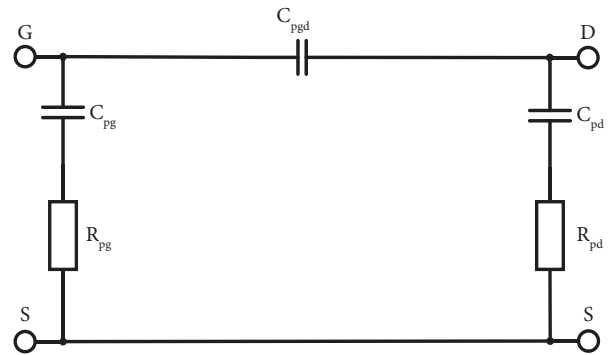


FIGURE 6: The equivalent circuit of the PAD structure.

Step 1: the S-parameter S_{DUT} of the device under different bias conditions is obtained by using the on-chip test system.

Step 2: strip the parallel parasitic parameters according to the following equation:

$$Y^{HEMT1} = Y^{DUT} - Y^{open}. \quad (10)$$

Formula (9) represents the stripping of parasitic parameters from admittance parameters of the device under test, and formula (5) represents the stripping of parallel parasitic parameters from impedance parameters of the short-test structure. Y^{HEMT1} represents the admittance parameter of the transistor under test after de-embedding.

TABLE 1: Results of parasitic parameter extraction.

Parameters	Units	Values
C_{pgd}	fF	0.0046
C_{pg}	fF	18.1273
C_{pd}	fF	17.2525
R_d	Ω	4.0713
R_g	Ω	2.2850
R_{pg}	Ω	45.54
R_{pd}	Ω	20.83
R_s	Ω	0.255
L_d	pH	117.332
L_g	pH	119.605
L_s	pH	47.663

Step 3: convert Y^{HEMT1} and Y^{short1} into corresponding impedance parameters Z^{HEMT1} and Z^{short1} and then subtract them to obtain impedance parameter Z^{HEMT} of the device under test after removing the influence of parasitic parameters:

$$Z^{\text{HEMT}} = Z^{\text{HEMT1}} - Z^{\text{short1}}. \quad (11)$$

Step 4: the YHEMT parameter of the transistor can be obtained by converting ZHEMT into impedance parameter.

Step 5: the intrinsic parameters of the device under test were calculated according to the following formulas:

$$\begin{aligned} C_{gd} &= -\frac{\text{Im}(Y_{12}^{\text{HEMT}})}{\omega}, \\ C_{gs} &= \frac{\text{Im}(Y_{11}^{\text{HEMT}} + Y_{12}^{\text{HEMT}})}{\omega}, \\ C_{ds} &= \frac{\text{Im}(Y_{22}^{\text{HEMT}} + Y_{12}^{\text{HEMT}})}{\omega}, \\ g_{ds} &= \frac{1}{\text{Re}(Y_{22}^{\text{HEMT}})}, \\ g_m &= \left| \text{Im}(Y_{21}^{\text{HEMT}}) - \text{Im}(Y_{12}^{\text{HEMT}}) \right|, \\ \tau &= -\frac{1}{\omega} \tan^{-1} \left[\frac{\text{Im}(Y_{11}^{\text{HEMT}} + Y_{12}^{\text{HEMT}})}{\text{Re}(Y_{11}^{\text{HEMT}} + Y_{12}^{\text{HEMT}})} \right]. \end{aligned} \quad (12)$$

4. Measurement and Discussion

The S-parameter measurements for model extraction and verification were made up from 0.5 GHz to 110 GHz using an Agilent E8361A network analyzer, with DC bias being supplied by an Agilent E5270A. All measurements were carried out on wafer using Cascade Microtech's Air-Coplanar Probes M150, with all instruments under IC CAP software control. The wafer probes were calibrated using line-reflect-match (LRM) calibration technology.

The parasitic capacitances extraction method proposed in this paper has been proved on wafer up to 110 GHz using GaN HEMTs with 0.15 μm gate length. In this paper, the GaN

TABLE 2: Extracted results for intrinsic capacitances under pinch-off bias condition.

Gate length (μm)	Im Y_{11}/ω (fF)	Im Y_{22}/ω (fF)
10	127.7	95.2
20	178.6	200.5
30	338.8	228.5
40	498.2	312.4
60	619.4	407.3

TABLE 3: Results of intrinsic parameter extraction, bias: $V_g = -5 \text{ V}$ and $V_d = 4 \text{ V}$.

Parameters	Units	Values
g_m	nS	9.113
C_{gs}	fF	94.362
R_i	Ω	1.139
C_{gd}	Ω	15.454
C_{ds}	Ω	59.896
R_{ds}	k Ω	4.982

TABLE 4: Results of intrinsic parameter extraction, bias: $V_g = 0 \text{ V}$ and $V_d = 8 \text{ V}$.

Parameters	Units	Values
g_m	mS	26.699
C_{gs}	fF	140.518
R_i	Ω	8.372
C_{gd}	Ω	13.663
C_{ds}	Ω	33.021
R_{ds}	Ω	481.778

TABLE 5: Results of intrinsic parameter extraction, bias: $V_g = -5 \text{ V}$ and $V_d = 0 \text{ V}$.

Parameters	Units	Values
g_m	nS	7.699
C_{gs}	fF	93.39
R_i	Ω	1.575
C_{gd}	Ω	22.817
C_{ds}	Ω	62.564
R_{ds}	k Ω	11.6875

HEMTs with $2 \times 10 \mu\text{m}$, $4 \times 20 \mu\text{m}$, $6 \times 30 \mu\text{m}$, $8 \times 40 \mu\text{m}$, and $8 \times 60 \mu\text{m}$ gate width (number of gate fingers \times unit gate width) and a comparison of the novel method with the conventional method are given.

The measured pinch-off cold-FET S-parameters for three different size HEMTs are firstly transformed to Y-parameters, and then the imaginary parts of Y-parameters can be extracted at low frequencies. The bias condition is $V_{gs} = -5 \text{ V}$ and $V_{ds} = 0 \text{ V}$. Under this bias condition, the whole network is in a cutoff state. The corresponding intrinsic capacitances under pinch-off bias condition are summarized in Table 2.

The values of substrate resistances can be extracted under bias of $V_{gs} = 0 \text{ V}$ and $V_{ds} = 0 \text{ V}$. Under this bias condition, the HEMT is already in saturation region. The extraction results of substrate resistances values are $R_{pd} = 45.54 \Omega$ and $R_{pg} = 20.83 \Omega$, respectively.

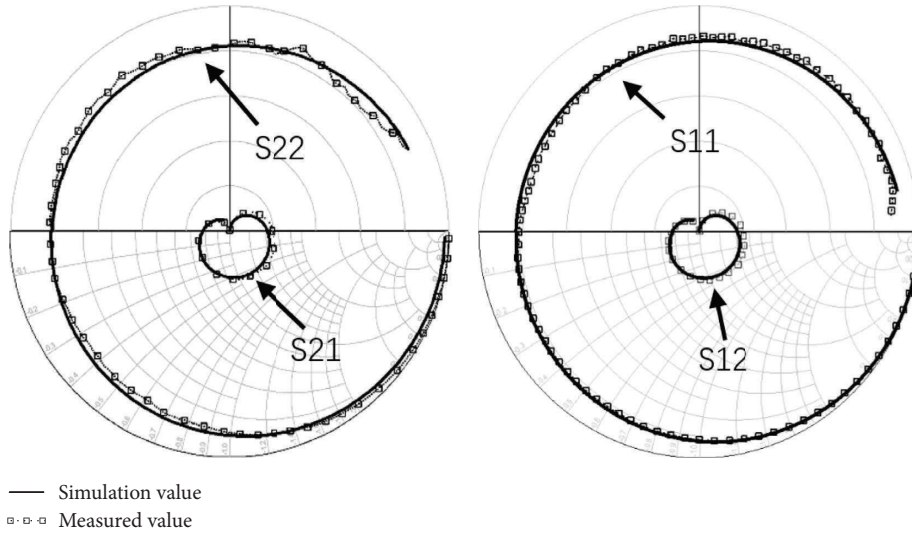


FIGURE 7: Measured (square) and simulated (line) S -parameters, bias: $V_g = -5$ V and $V_d = 4$ V.

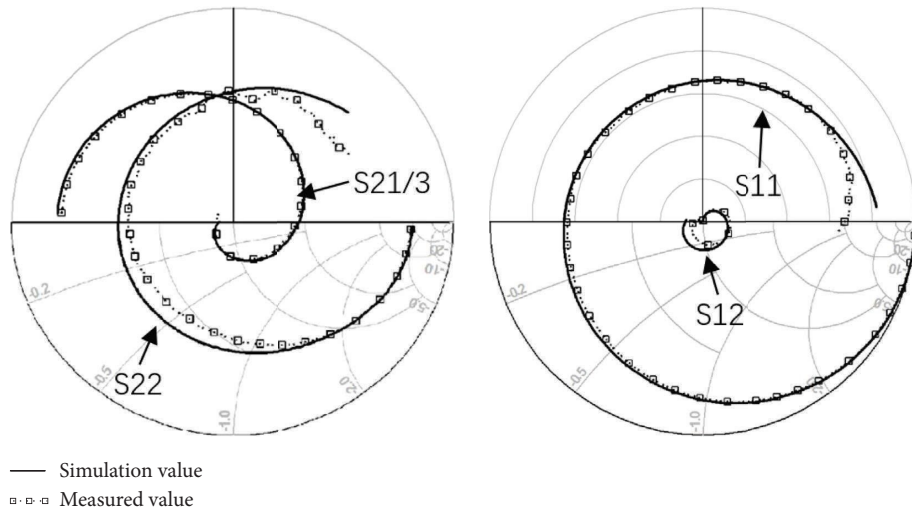


FIGURE 8: Measured (square) and simulated (line) S -parameters, bias: $V_g = 0$ V and $V_d = 8$ V.

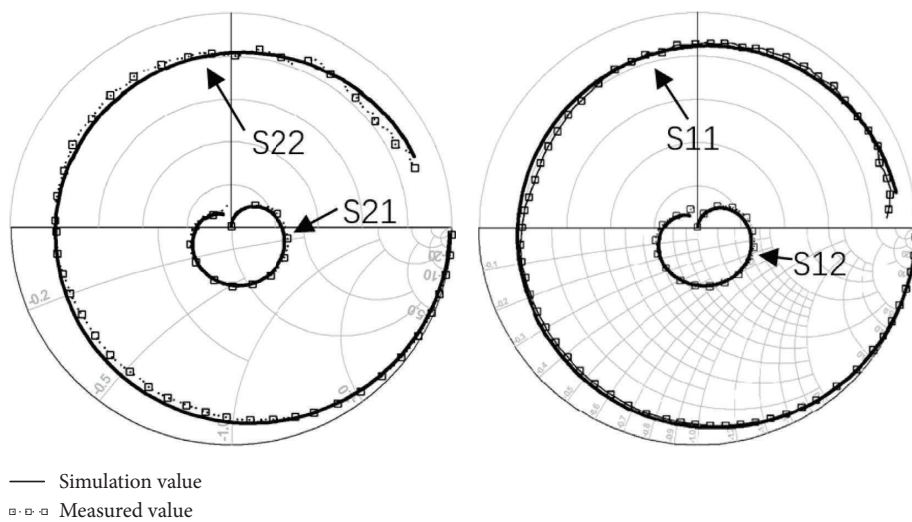


FIGURE 9: Measured (square) and simulated (line) S -parameters, bias: $V_g = -5$ V and $V_d = 0$ V.

The equivalent circuit was constructed in the Keysight ADS software; a set of bias in the saturation region ($V_g = 0\text{ V}$ and $V_d = 8\text{ V}$) and the cutoff region ($V_g = -5\text{ V}$ and $V_d = 4\text{ V}$), respectively, is for verification. The obtained parasitic parameters and intrinsic parameters were substituted into the model as initial values for iterative optimization. The final results are shown in Tables 3–5.

5. Experimental Verification

Figures 7–9 show the comparison of the reflection and transmission co-efficients of simulations and measurements of the devices under the different bias in the frequency range of 0.5–110 GHz. It is observed from the figure that relatively good agreement between measured and simulated data can be achieved. Good agreement has been obtained between the modeled and measured S-parameters to verify the improved parameter extraction approach in this article.

6. Conclusions

In this paper, an improved method is used to extract the parasitic resistances of the gate, source, and drain when extracting the parameters of the small-signal equivalent circuit model of the GaN HEMTs. The proposed method without the open-test structure is compared with the traditional COLD-FET capacitance extraction method. The accuracy and effectiveness of the method based on the size scalable model in the extraction of parasitic inductances are proved. The simulated S-parameters are in good agreement with the measured S-parameters in the frequency range up to 110 GHz.

Data Availability

The simulation and test data used to support the findings of this study are included within the figure files and can be obtained by contacting the author (chengjl@jou.edu.cn).

Conflicts of Interest

The authors declare that there are no conflicts of interest regarding the publication of this paper.

Acknowledgments

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